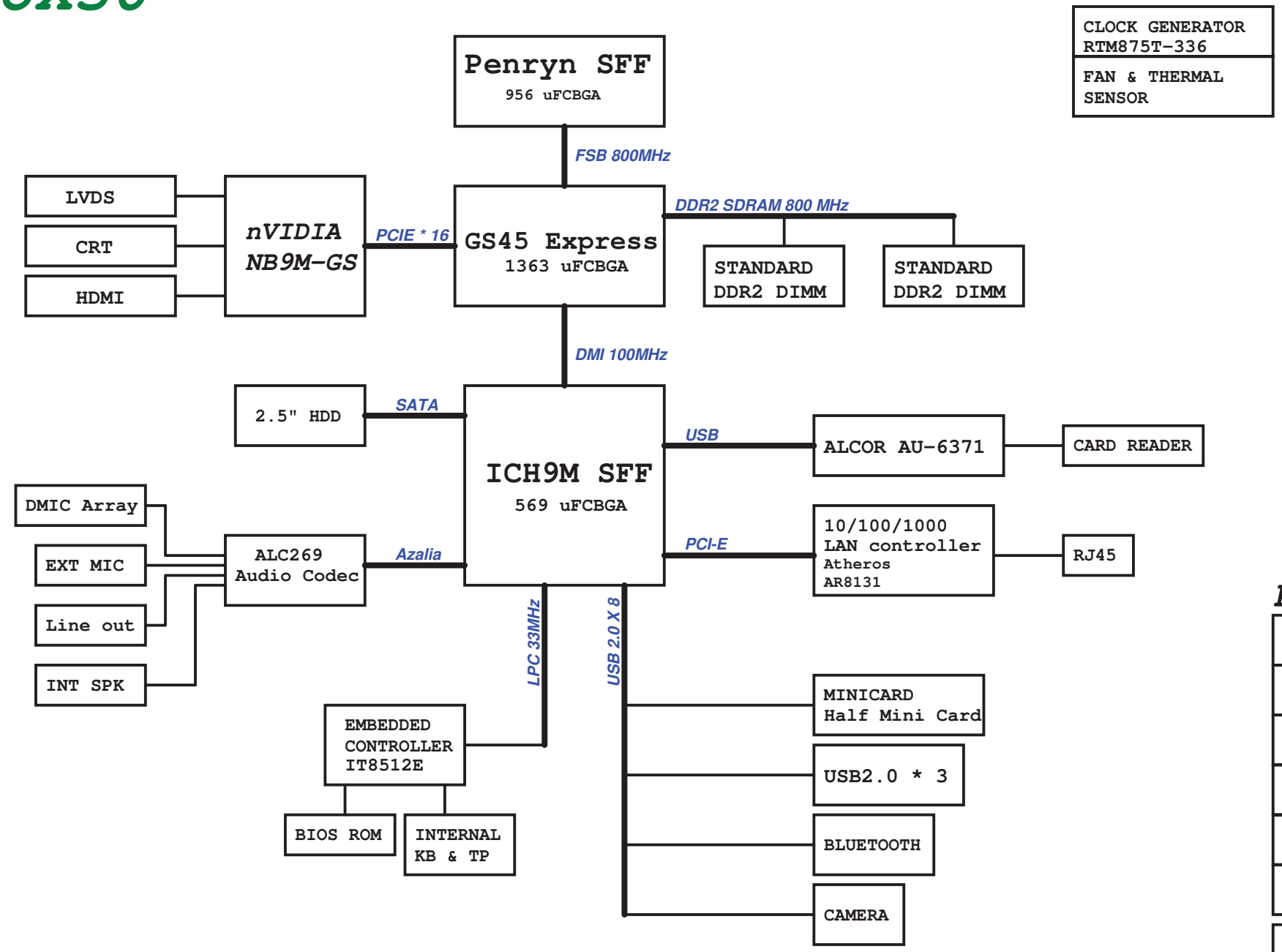
UX50



CLOCK GENERATOR
RTM875T-336

FAN & THERMAL
SENSOR

POWER

- VCORE
- SYSTEM
- I/O_1.5VS & 1.05VS
- I/O_DDR & VTT
- I/O_ +1.8VS
- CHARGER
- LCD DRIVER

<Variant Name>

ASUSTeK COMPUTER INC

Title : Block diagram

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 1 of 97

UX50 SCHEMATIC Revision 1.0

PAGE	Content

SYSTEM PAGE REF.

PAGE	Content

POWER PAGE REF.

<Variant Name>

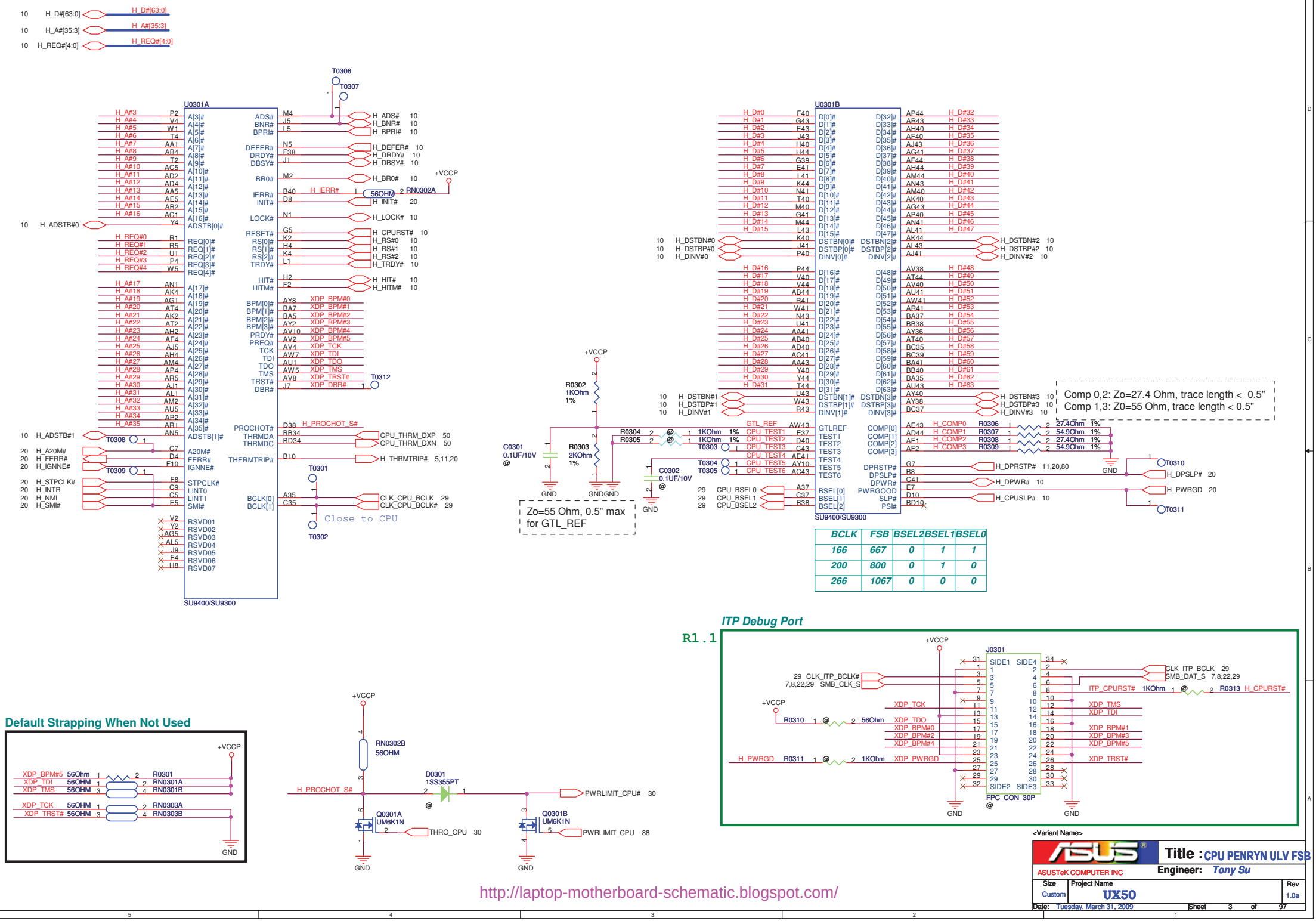
ASUSTeK COMPUTER INC

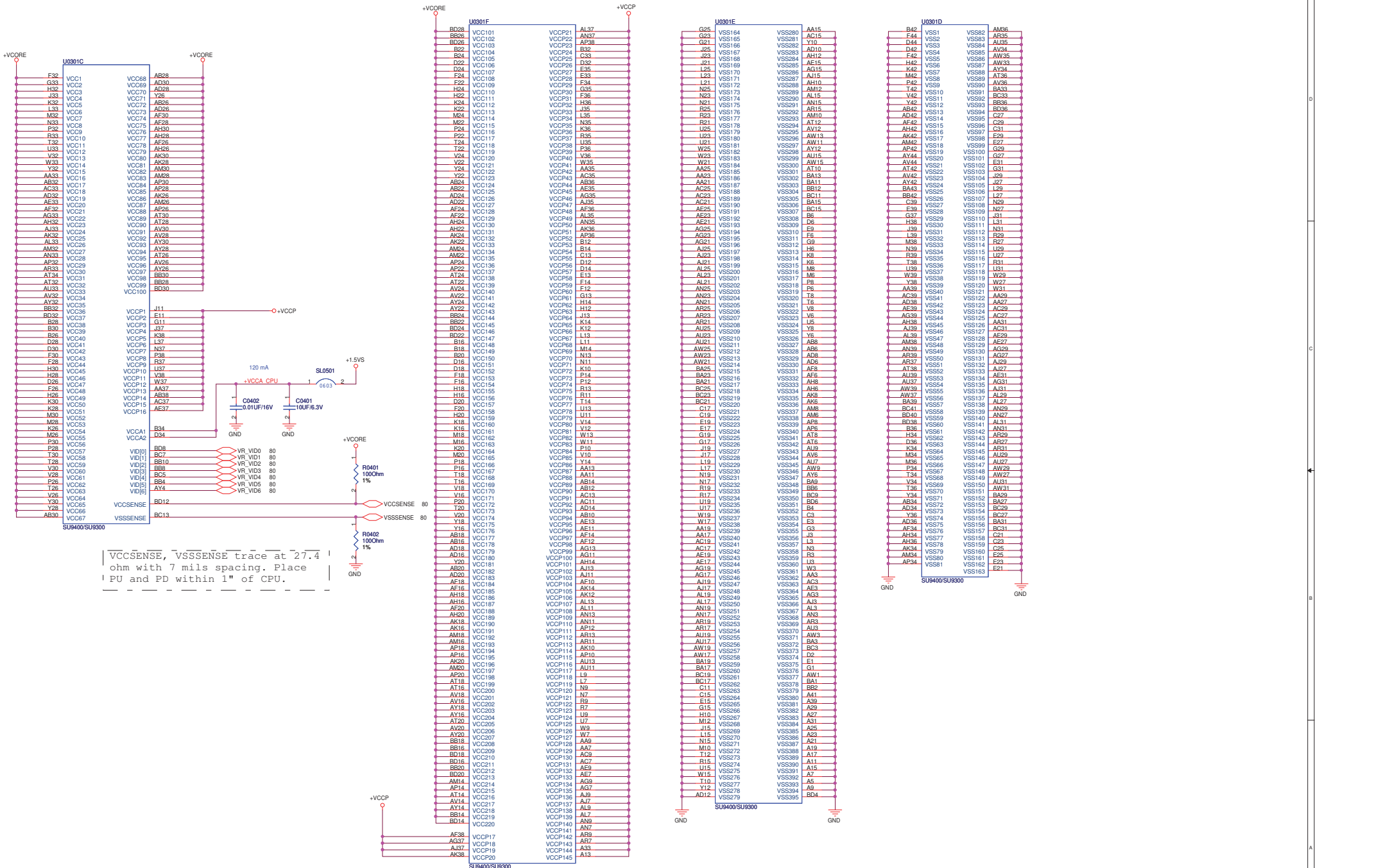
Title : PAGE REF.

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 2 of 97





<Variant Name>

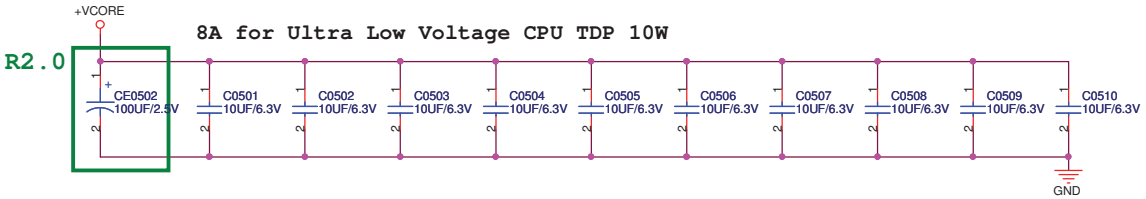
ASUSTeK COMPUTER INC

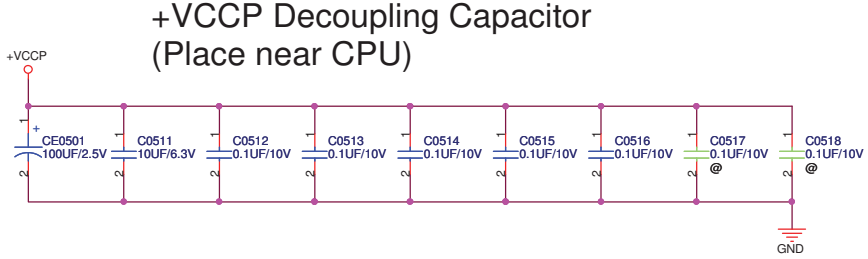
Title : CPU PENRYN ULV POWER

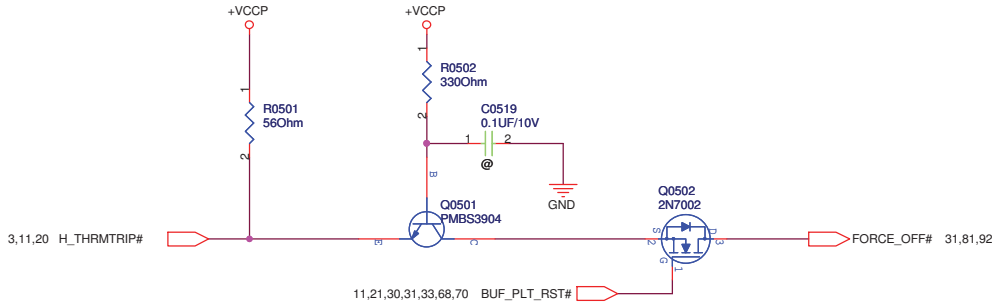
Engineer: Tony Su

Size	Project Name	Rev
C	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 4 of 97







Decoupling guide from Intel

VCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	* 12pcs
	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU CAPACITORS

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 5 of 97

<Variant Name>

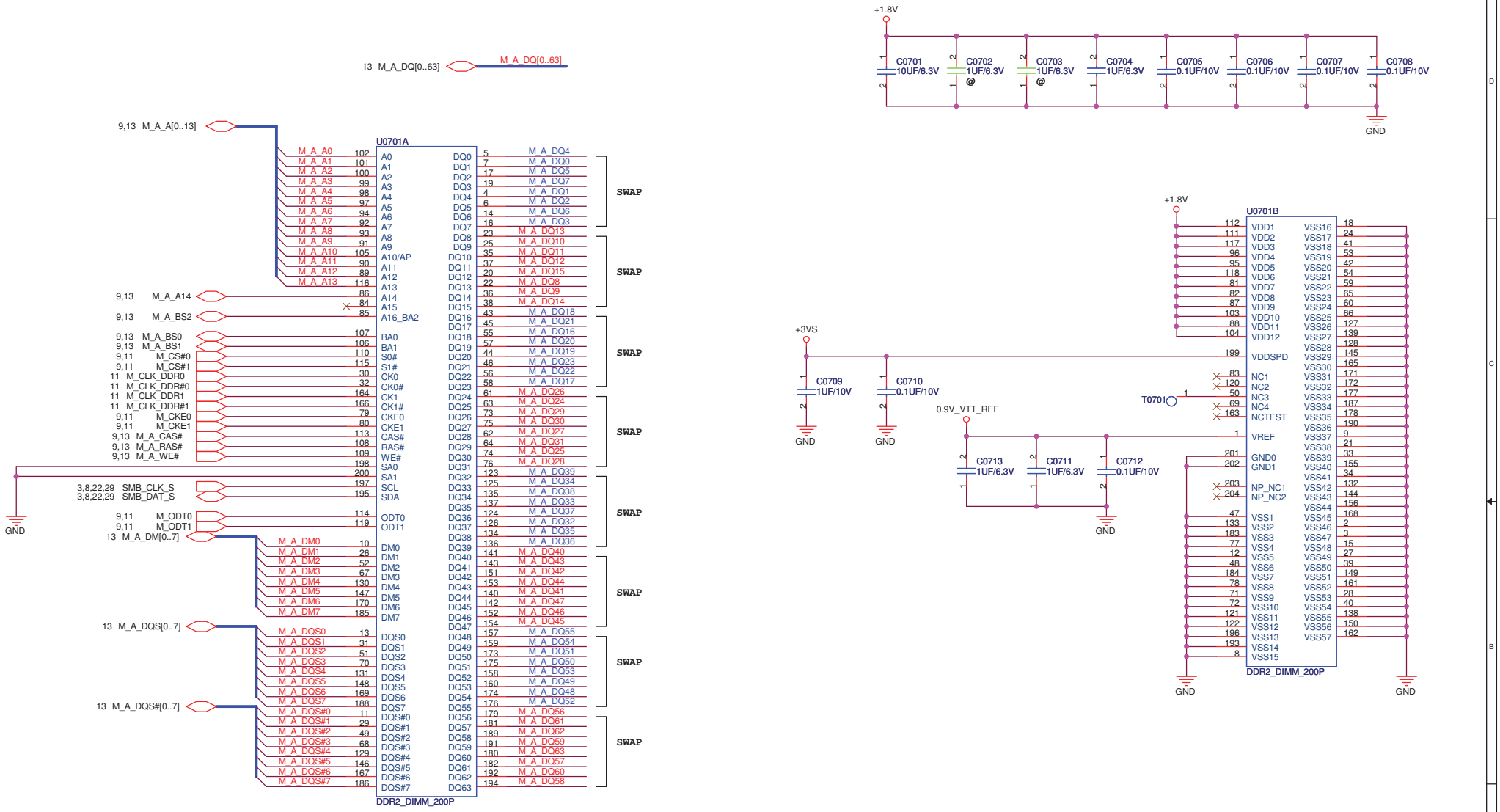
Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 6 of 97



PN : 12G02512200Y(STD Type)

<Variant Name>

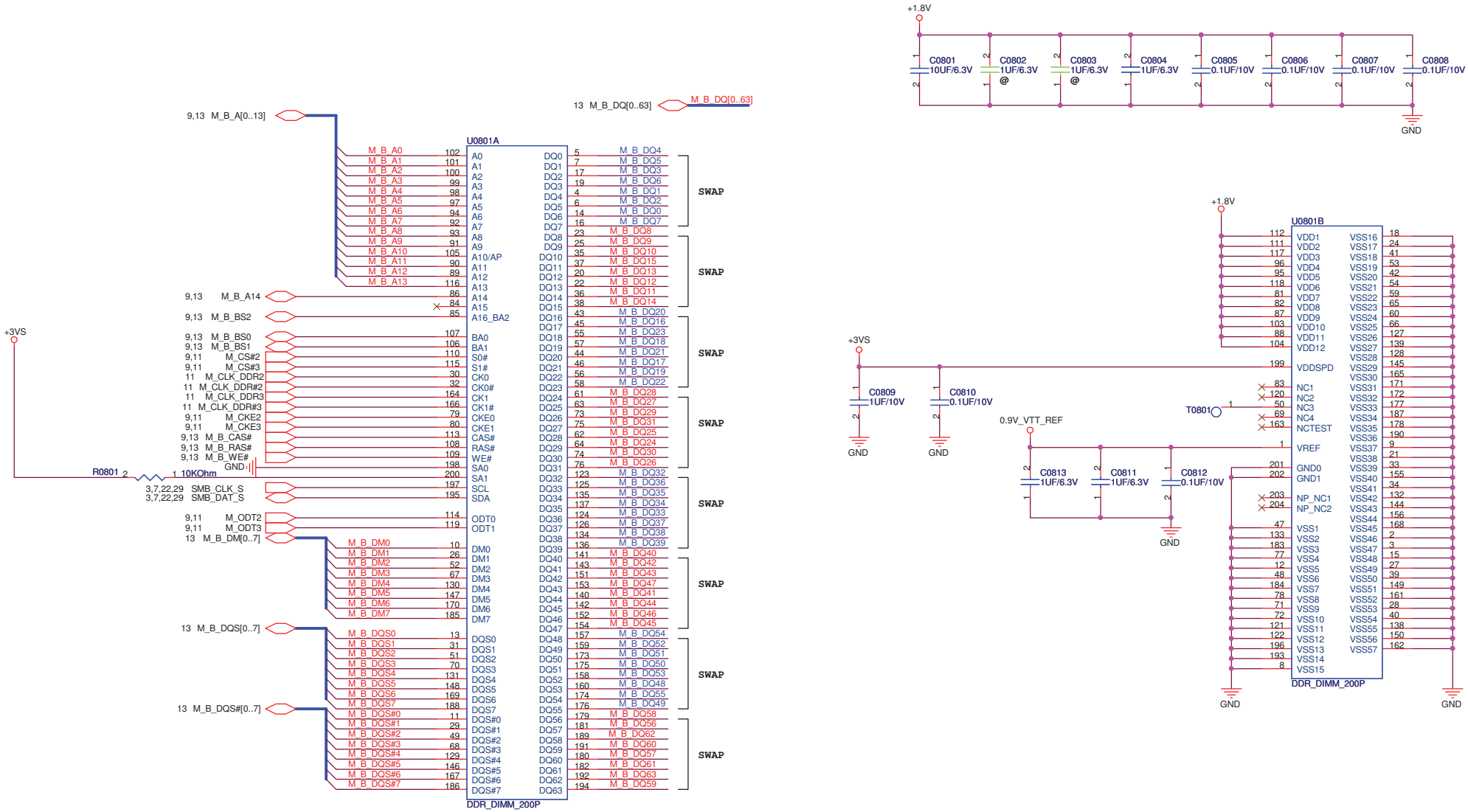
Title : R2 SO-DIMM CHANNEL A

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 7 of 97



PN: 12G02512200G(REV. Type)

<Variant Name>

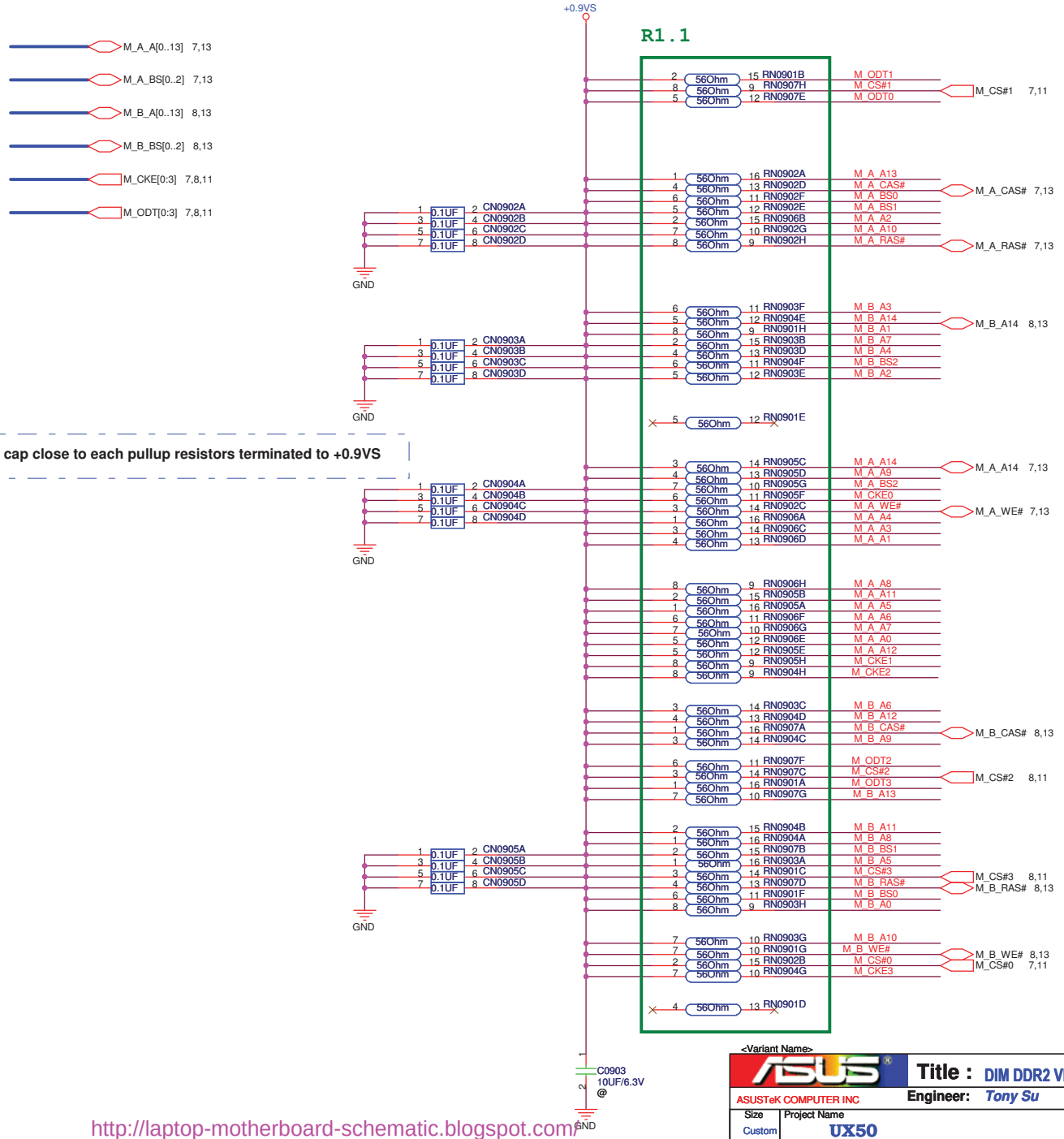
ASUSTeK COMPUTER INC

Title: DDR SP-DIMM CHANNEL B

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 8 of 97



<variant_name>

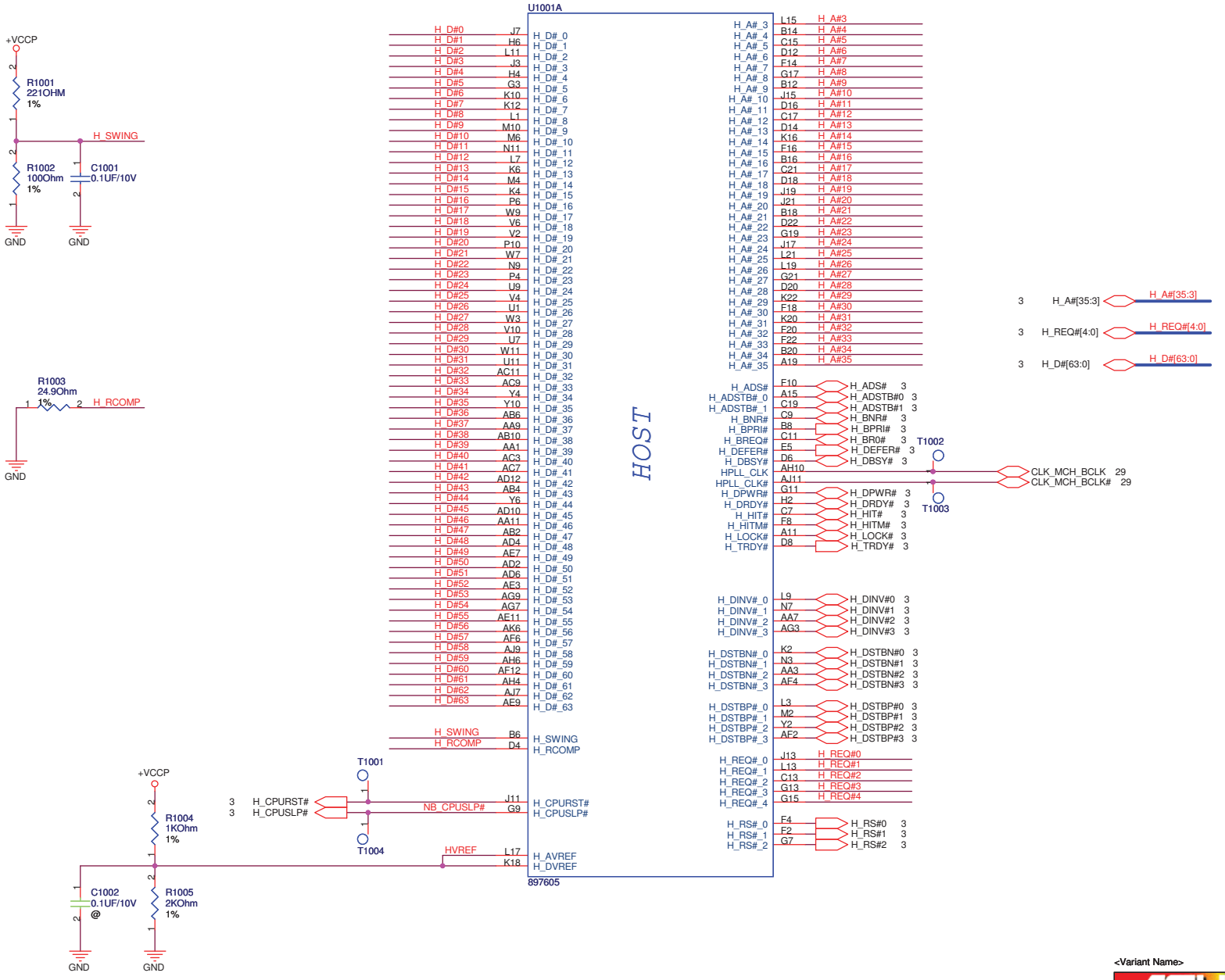
ASUSTeK COMPUTER INC

Title : DIM DDR2 VREF

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 9 of 97



<Variant Name>

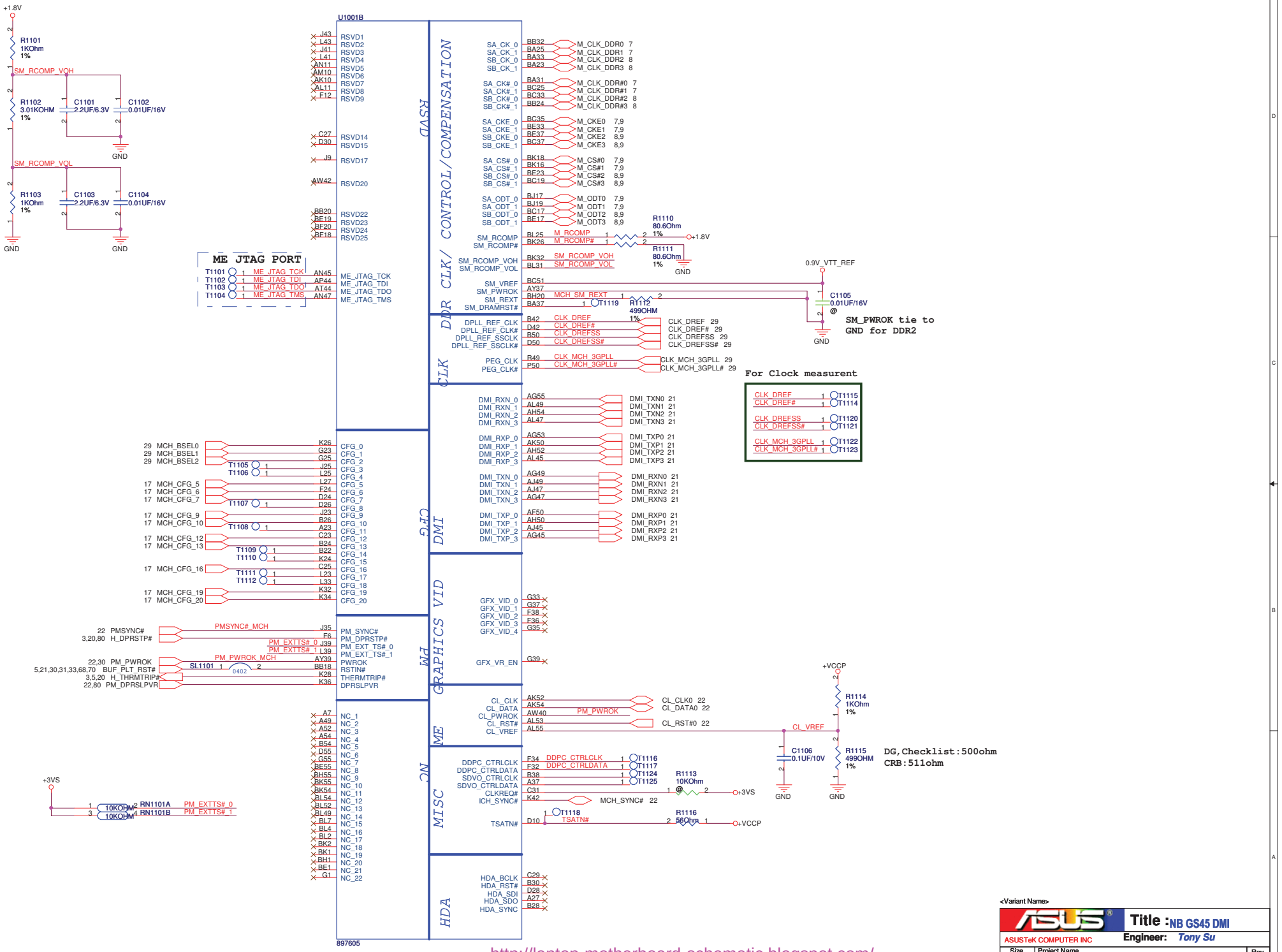
Title : NB GS45 HOST

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 10 of 97



<Variant Name>

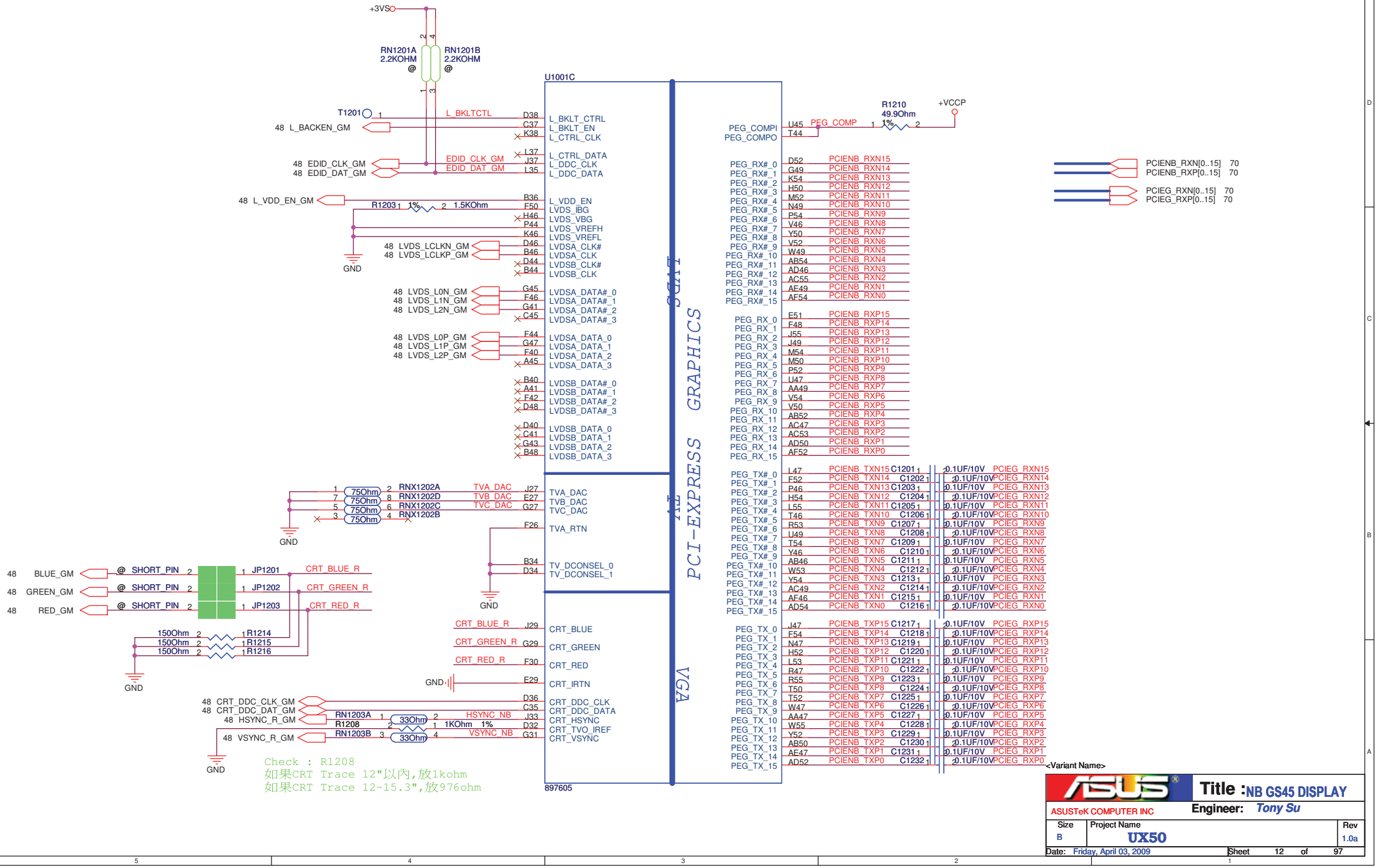
ASUSTeK COMPUTER INC

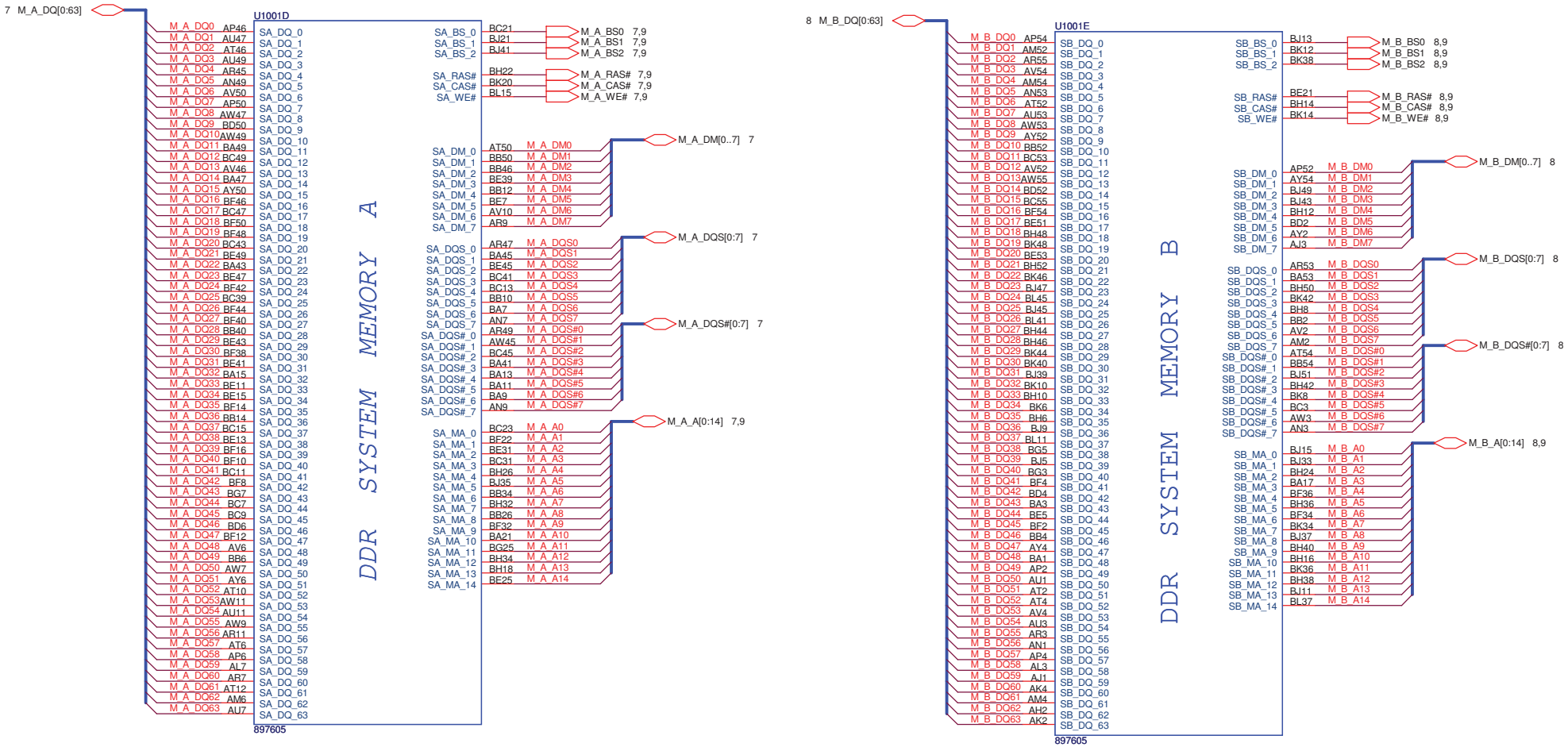
Title : NB GS45 DMI

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 11 of 97





<Variant Name>

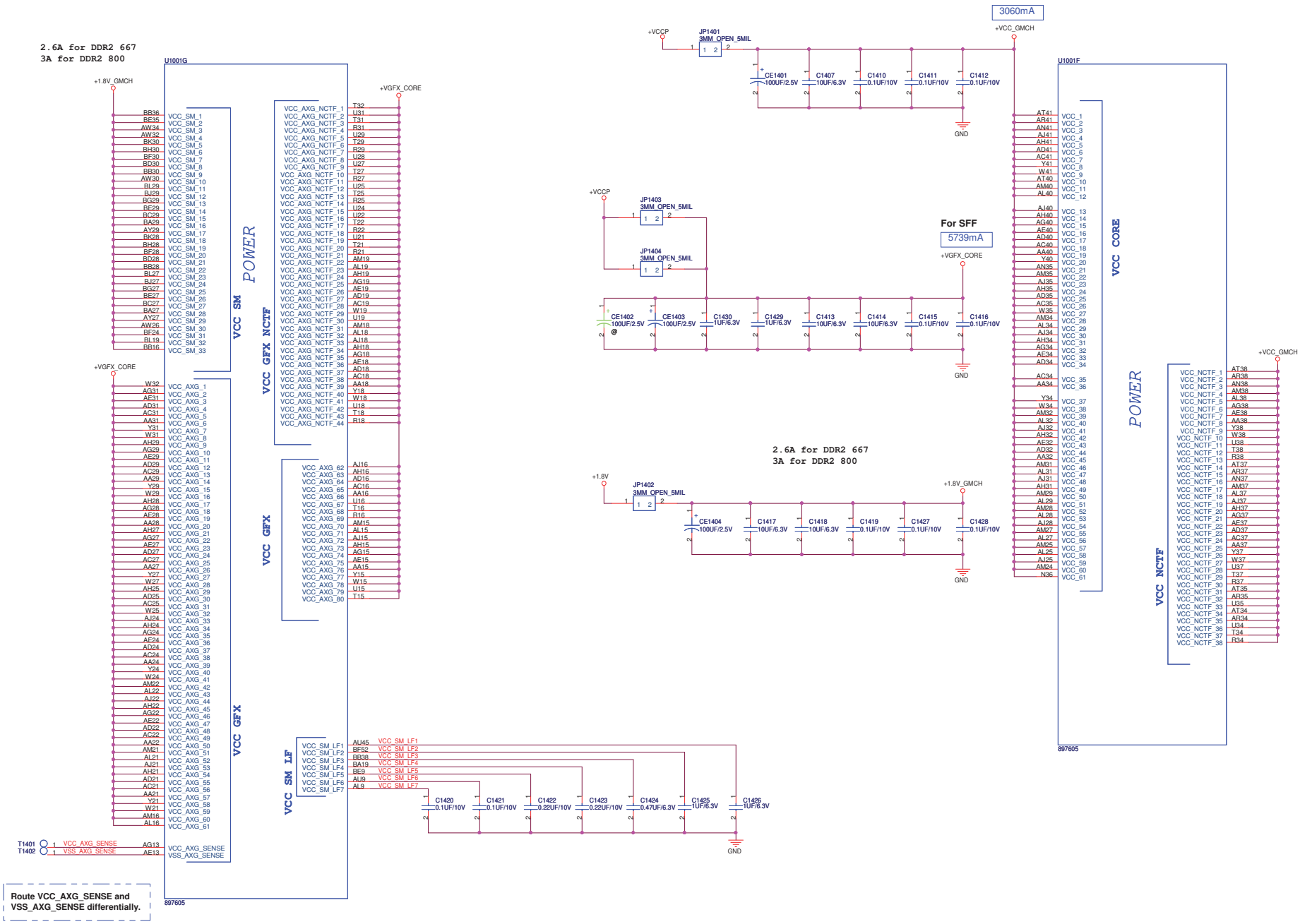
ASUSTeK COMPUTER INC

Title : NB GS45 DDR3 BUS

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 13 of 97



<Variant Name>

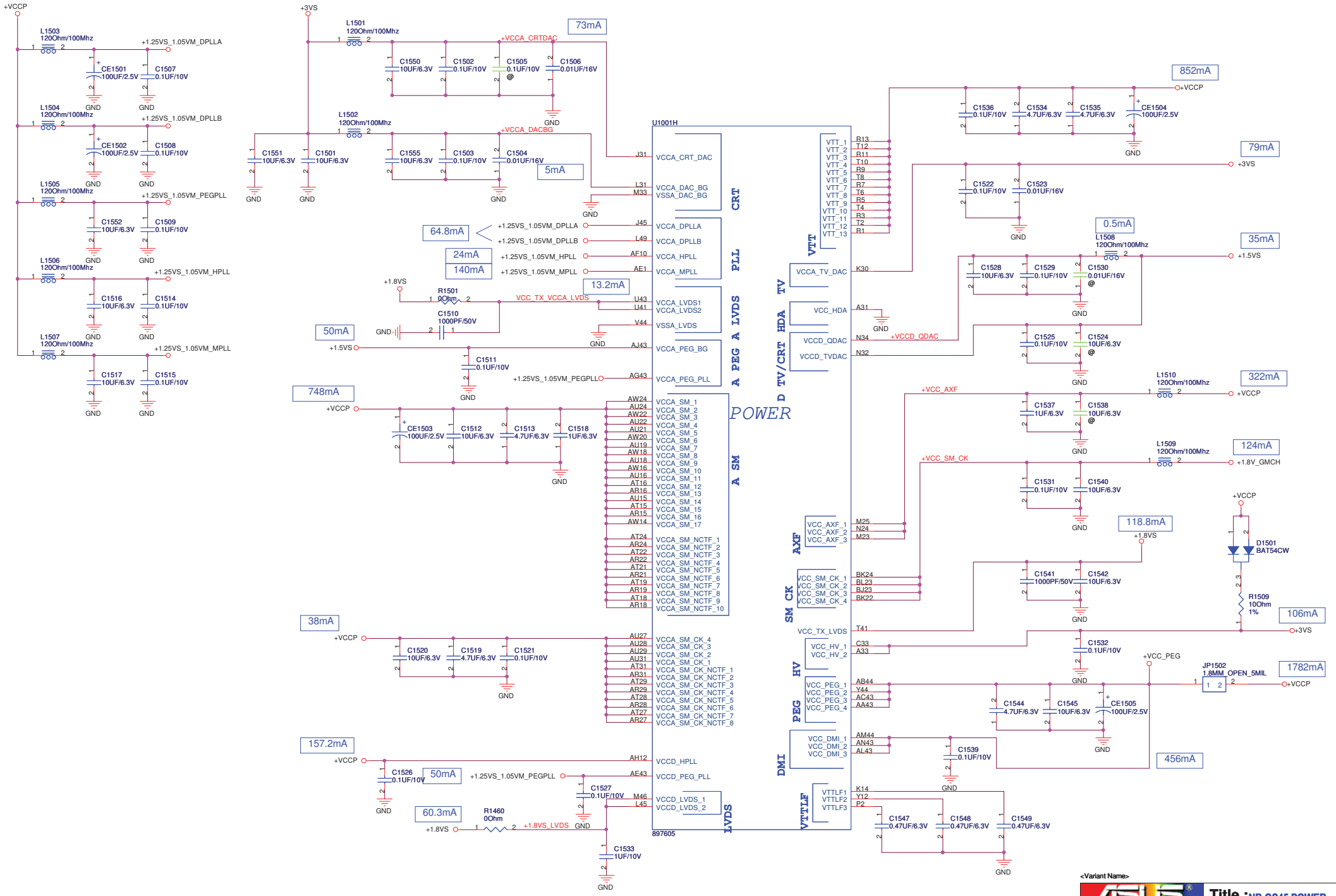
ASUSTeK COMPUTER INC

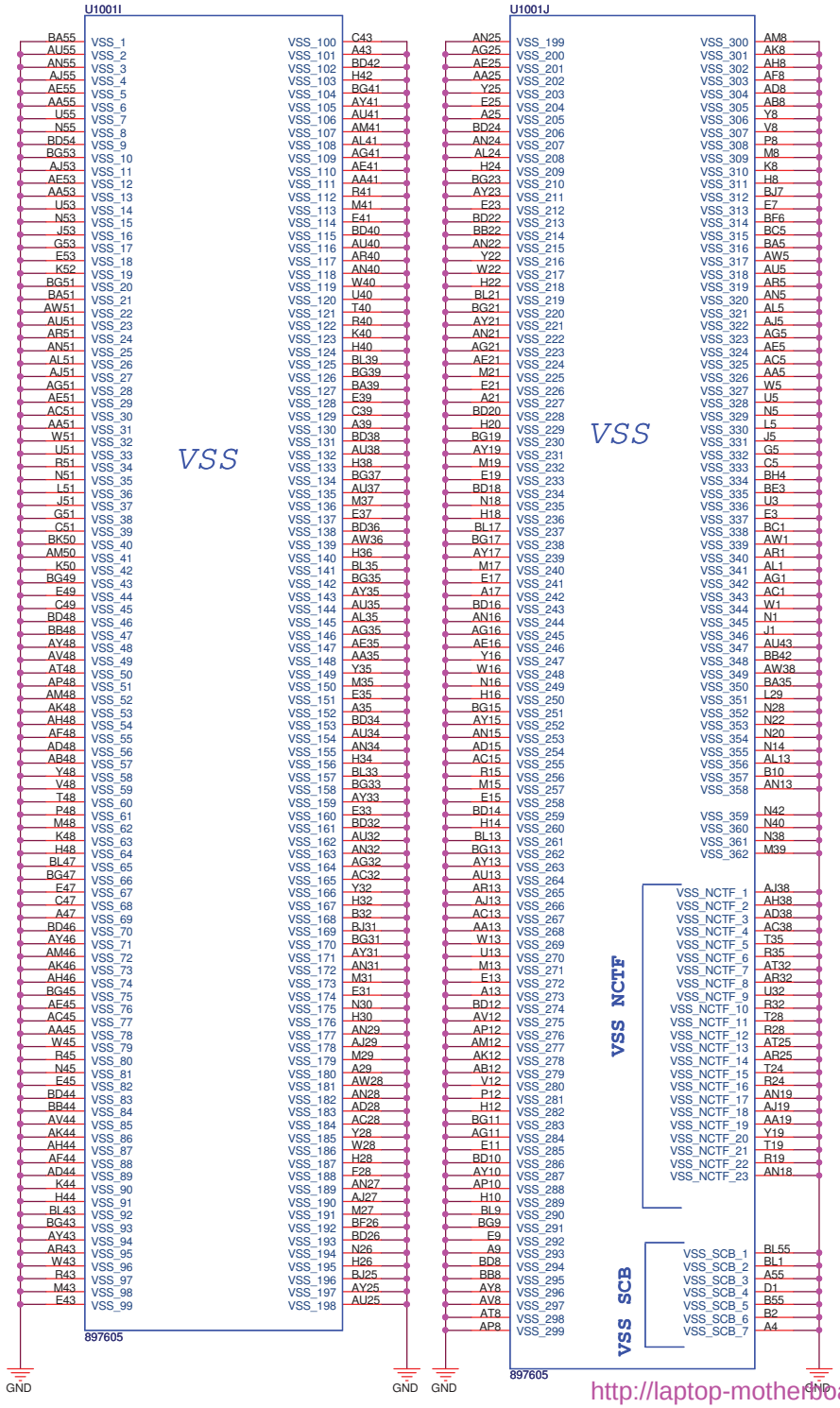
Title : NB GS45 POWER

Engineer: Tony Su

Size	Project Name	Rev
C	UX50	1.0a

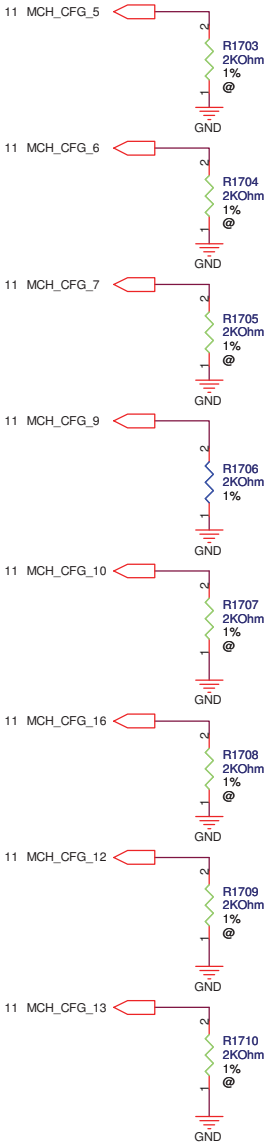
Date: Tuesday, March 31, 2009 Sheet 14 of 97





<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 GND	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 16 of 97	



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

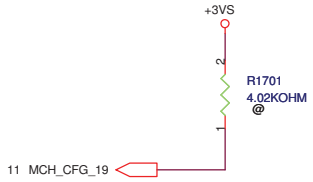
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

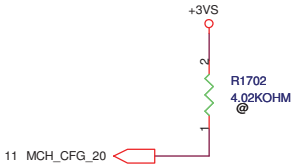
CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 STRAPPING	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Monday, April 06, 2009	Sheet 17 of 97	

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
C	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 18 of 97

<Variant Name>

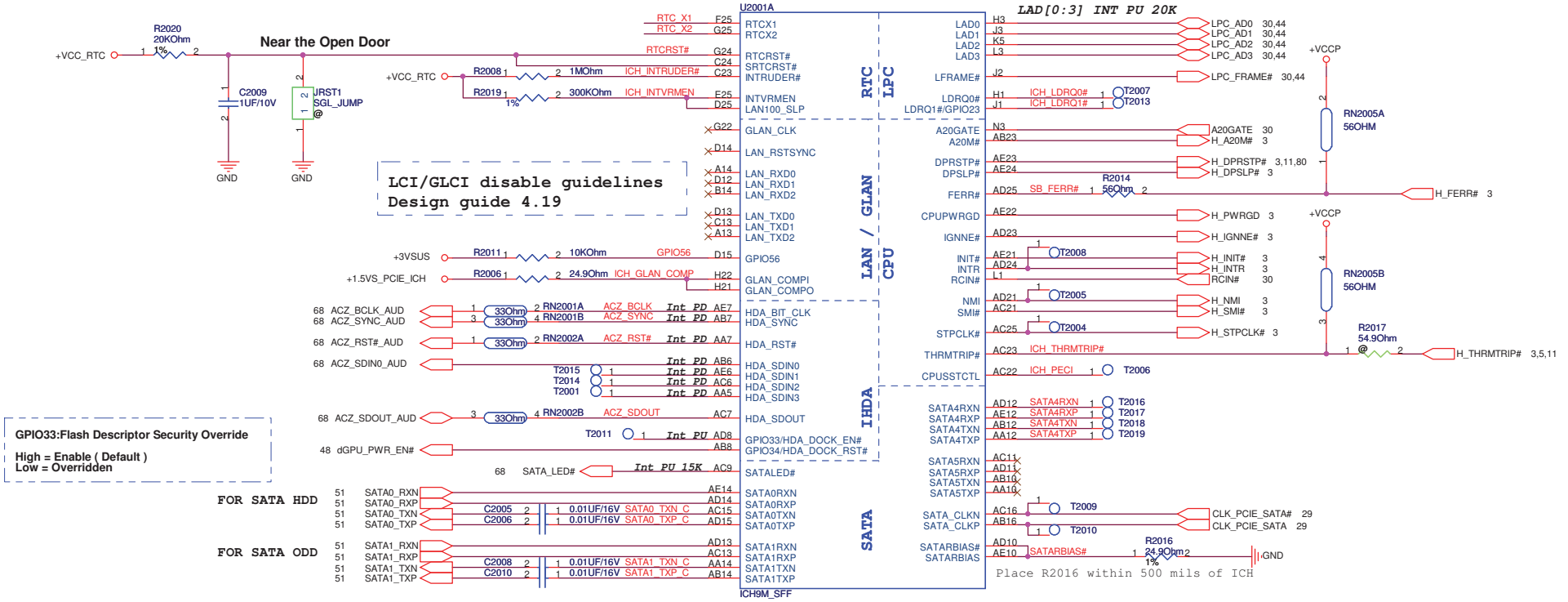
Title :

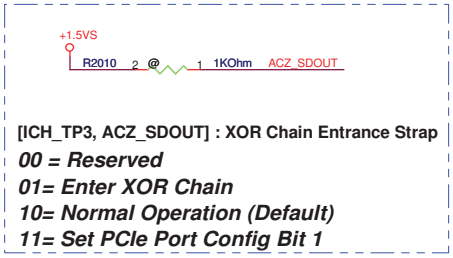
ASUSTeK COMPUTER INC

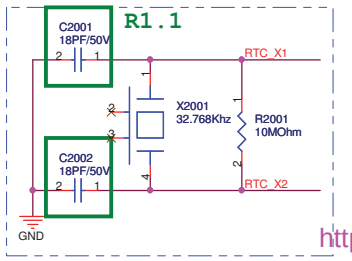
Engineer: Tony Su

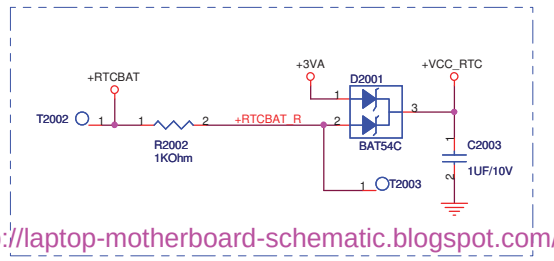
Size	Project Name	Rev
A	UX50	1.0a

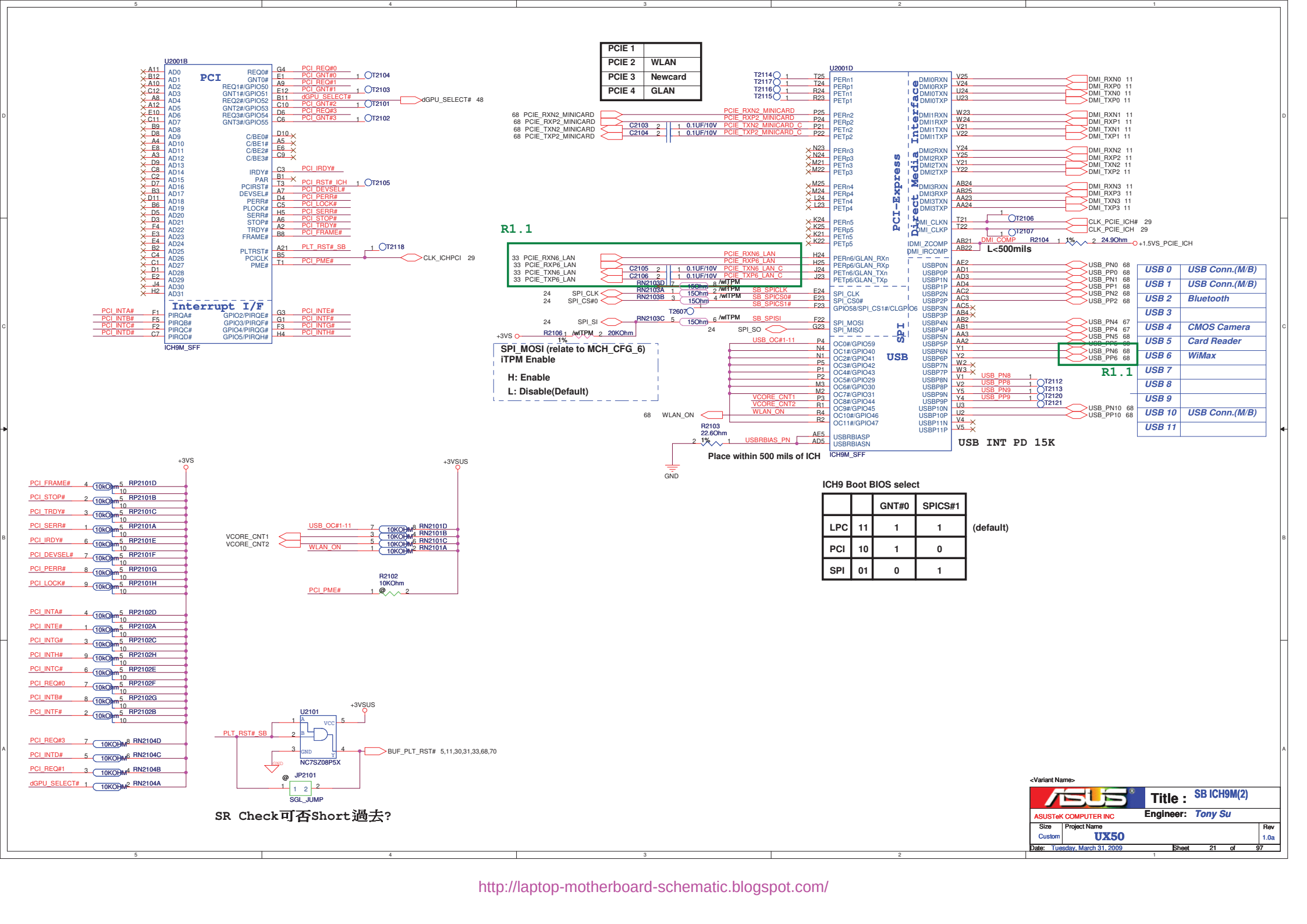
Date: Tuesday, March 31, 2009 Sheet 19 of 97

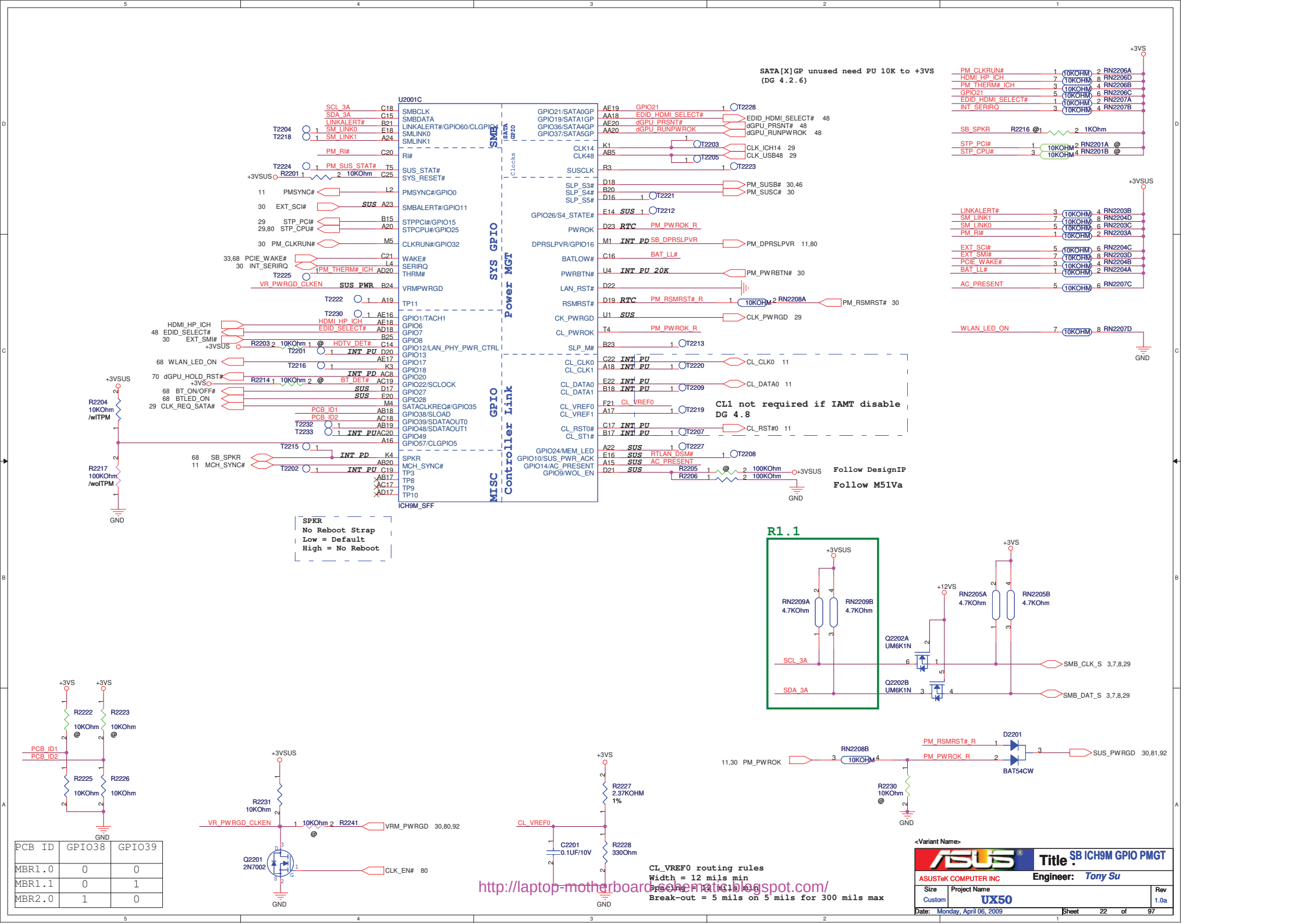


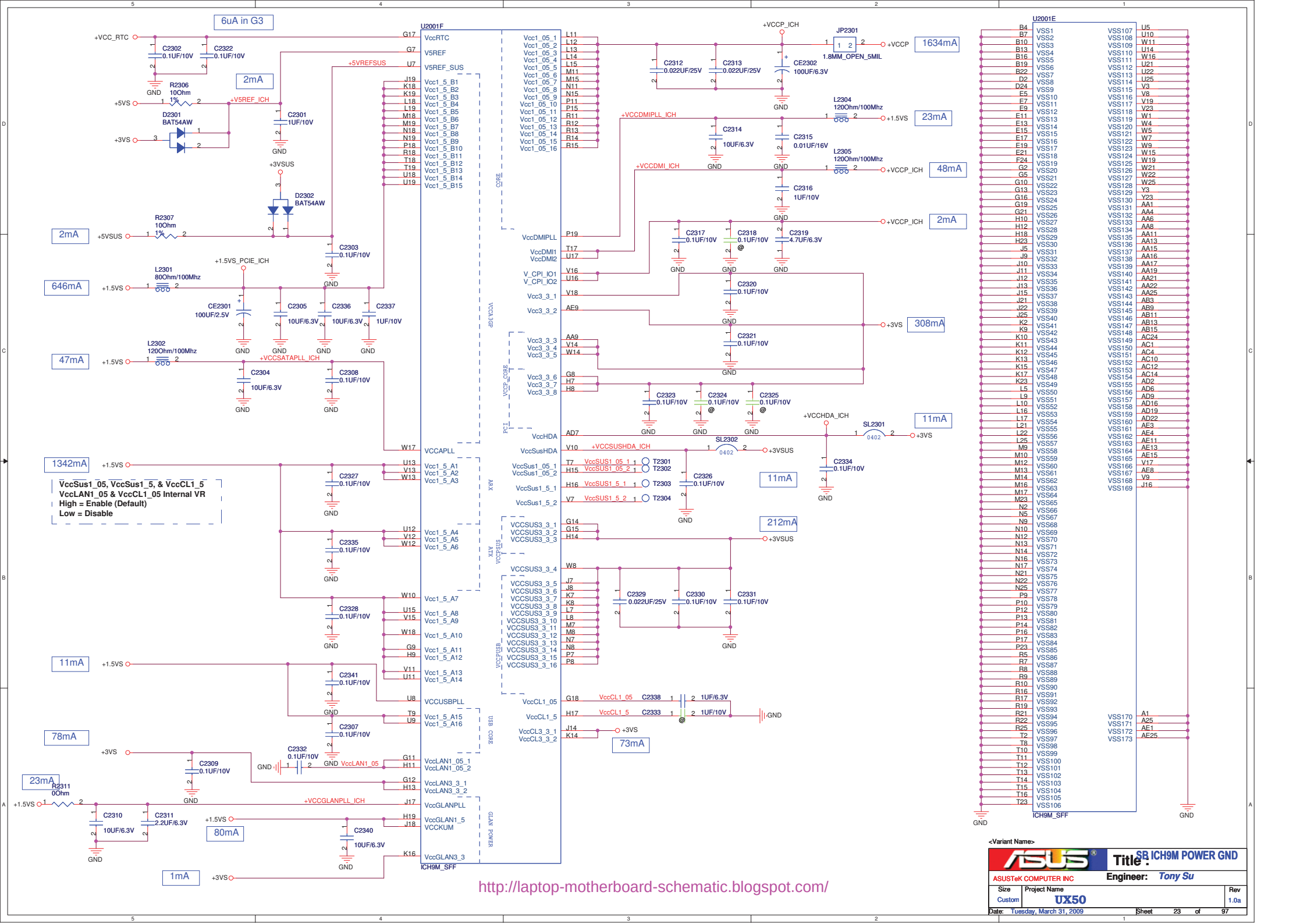


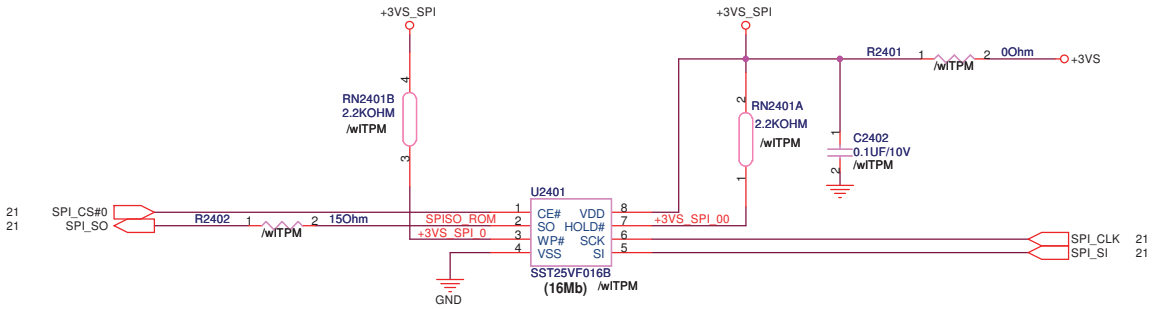







U2001C
ICH9M_SFF
SMB
GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA[X]GP unused need PU 10K to +3VS
(DG 4.2.6)
CL1 not required if IAMT disable
DG 4.8
Follow DesignIP
Follow M51Va
SPKR
No Reboot Strap
Low = Default
High = No Reboot
R1.1
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max
PCB ID | GPIO38 | GPIO39
MBR1.0 | 0 | 0
MBR1.1 | 0 | 1
MBR2.0 | 1 | 0
SB ICH9M GPIO PMGT
ASUSTeK COMPUTER INC
Engineer: Tony Su
Project Name: UX50
Rev: 1.0a
Date: Monday, April 06, 2009
Sheet 22 of 97
http://laptop-motherboard-schematic.blogspot.com/





FOR iTPM

<Variant Name>

ASUSTeK COMPUTER INC

Title : SB ICH9M SPI ROM & HDCP

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 24 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 25 of 97

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 26 of 97	

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 27 of 97

<Variant Name>

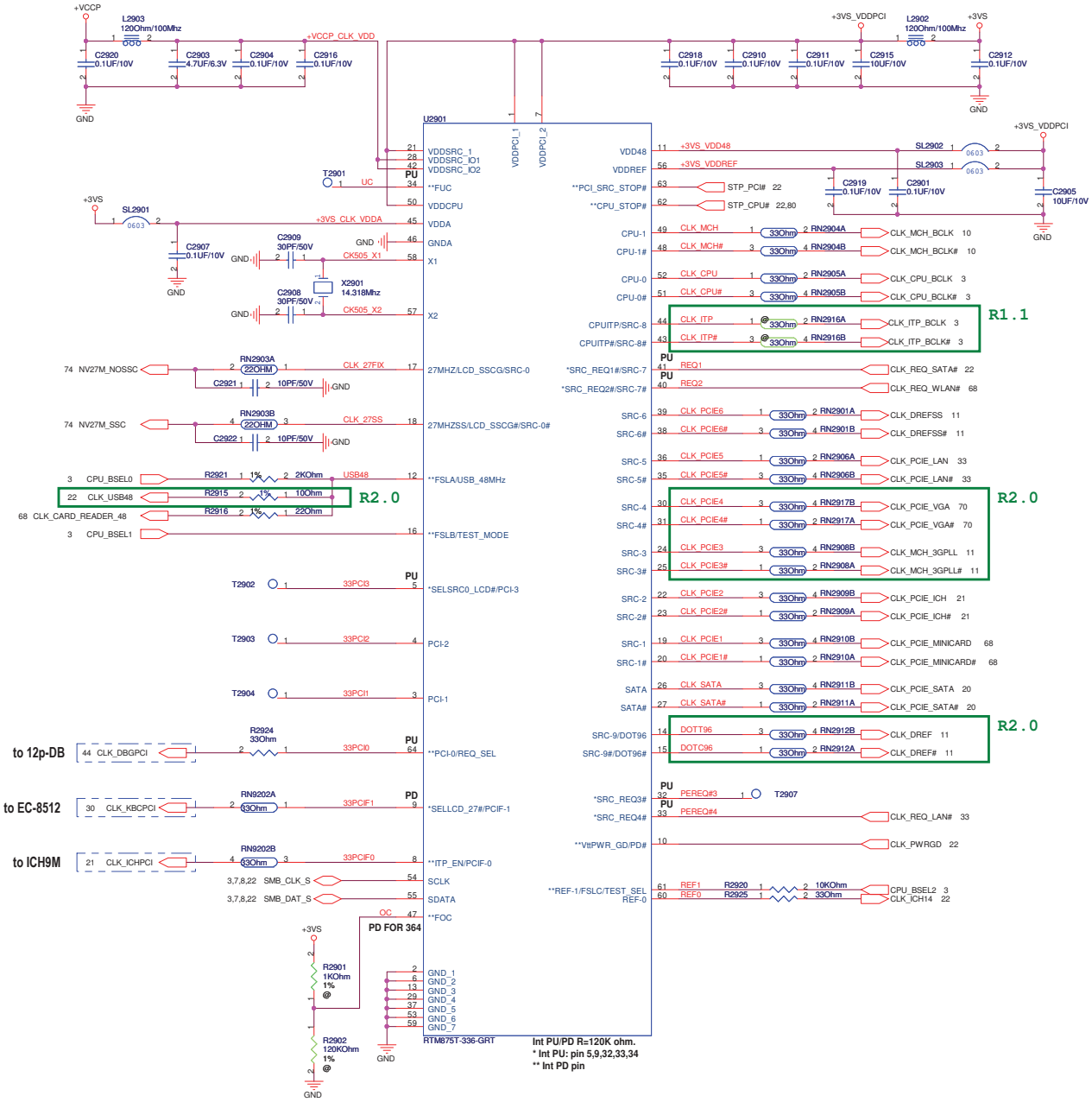
Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 28 of 97



Latched Input Select

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9	27FIX/SS
	SELLCD_27#=1	DOT96	LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	DOT96	27FIX/SS
	SELLCD_27#=1	DOT96	PCIEX0

Decide pin 43/44

0 = SRC CLK
1 = CPU_ITP CLK

(Pin8) ITP_EN — 33PCIF0 — 10KOHM — RN2913B

Decide pin 17/18
96MHz (Non - SSC)
100MHz SSC

0 = LCDCLK
1 = PCIEX

(Pin5) SELPCIEX0_LCD# — 33PCI3 — RN2914A 10KOHM — +3VS

Decide pin 40/41

0 = PCIECLK
1 = PEREQ#

(Pin64) REQ_SEL# — 33PCI0 — 10KOHM — RN2914B — +3VS

Decide pin 17/18

SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS

SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0

(Pin9) — 33PCIF1 — 10KOHM — RN2913A

3 CPU_BSEL0 — R2918 1KOhm — MCH_BSEL0 11
3 CPU_BSEL1 — R2919 1KOhm — MCH_BSEL1 11
3 CPU_BSEL2 — R2917 1KOhm — MCH_BSEL2 11

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

<Variant Name>

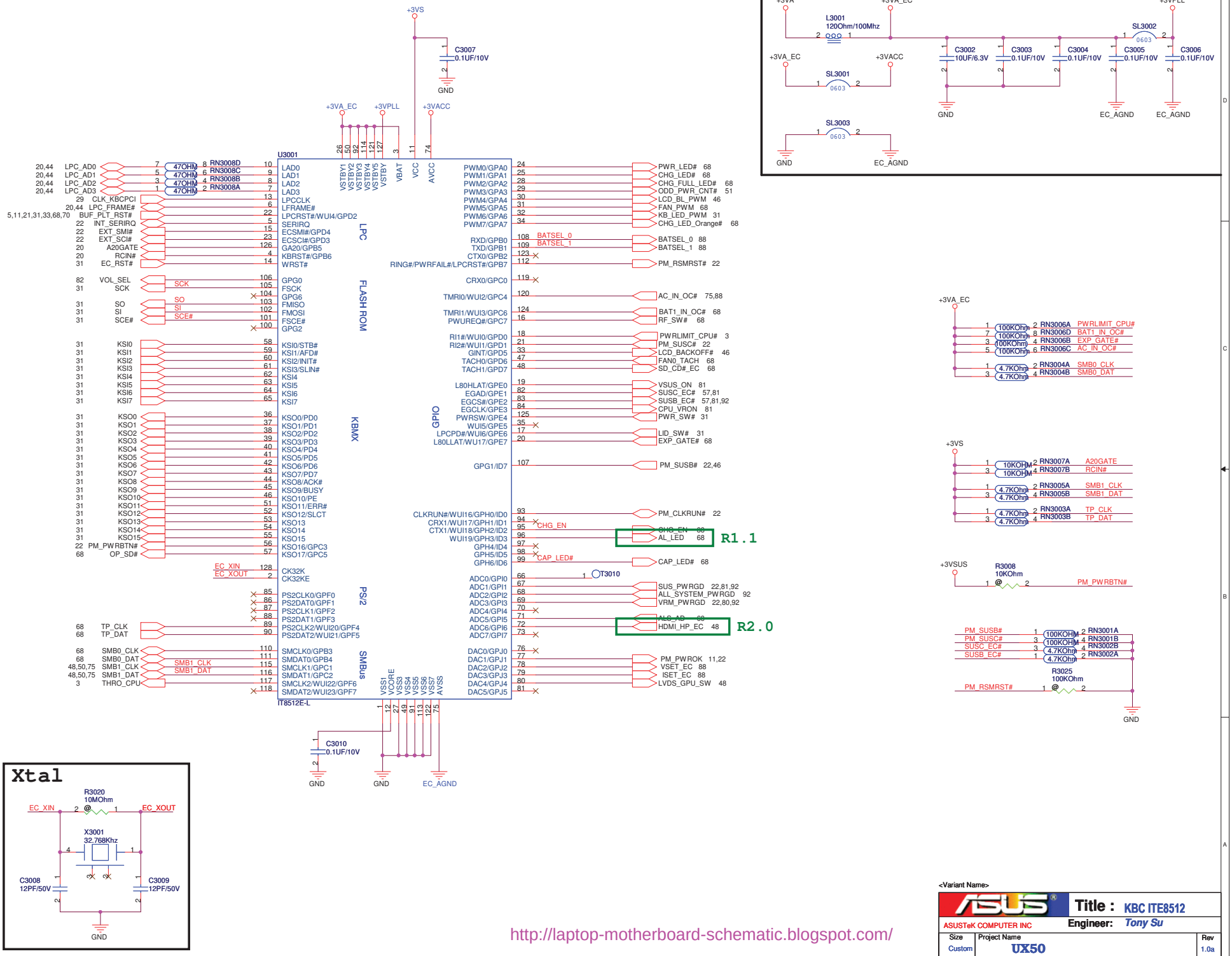
ASUSTeK COMPUTER INC

Title: CLK RTM875T-336-GRT

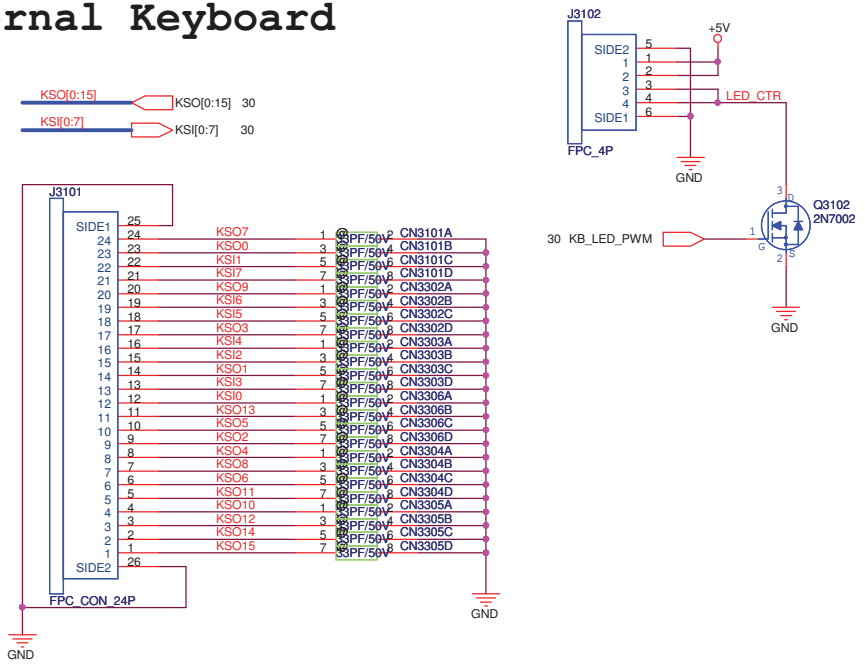
Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

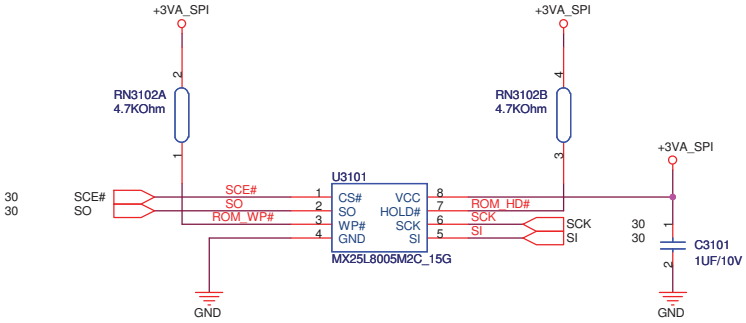
Date: Wednesday, April 01, 2009 Sheet 29 of 97



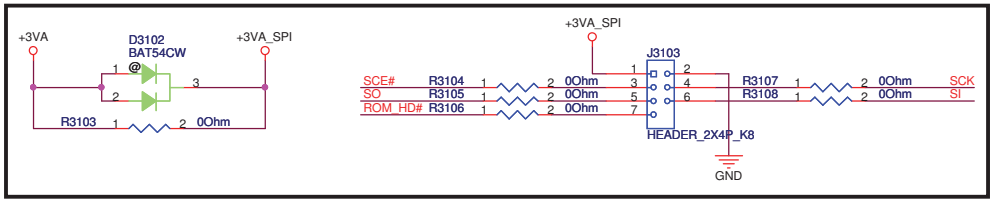
Internal Keyboard



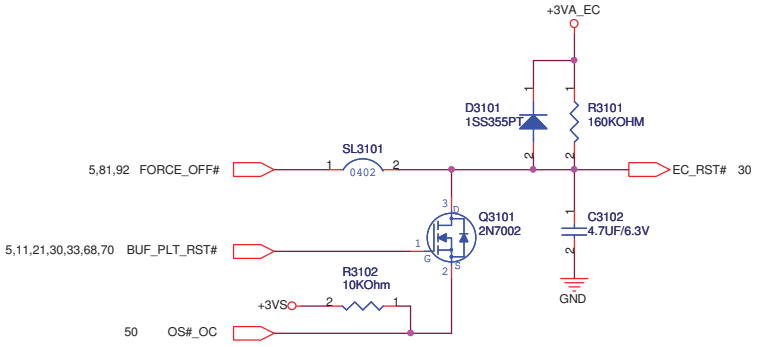
8Mb SPI ROM



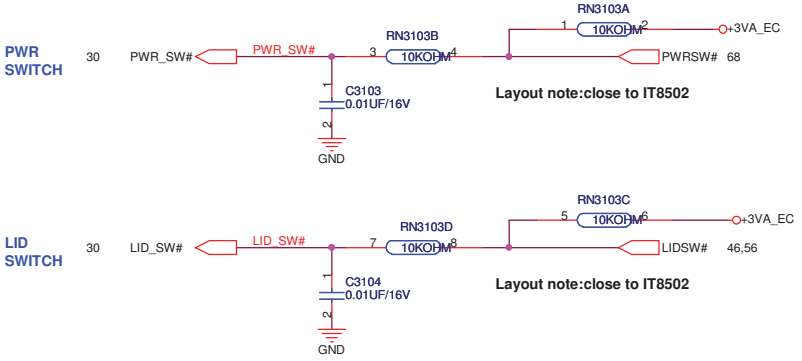
For SPI Flash Debug



EC RST



For Switch



<Variant Name> ROM FLASH ROM TOUCH PAD KB

ASUSTeK COMPUTER INC

Title :

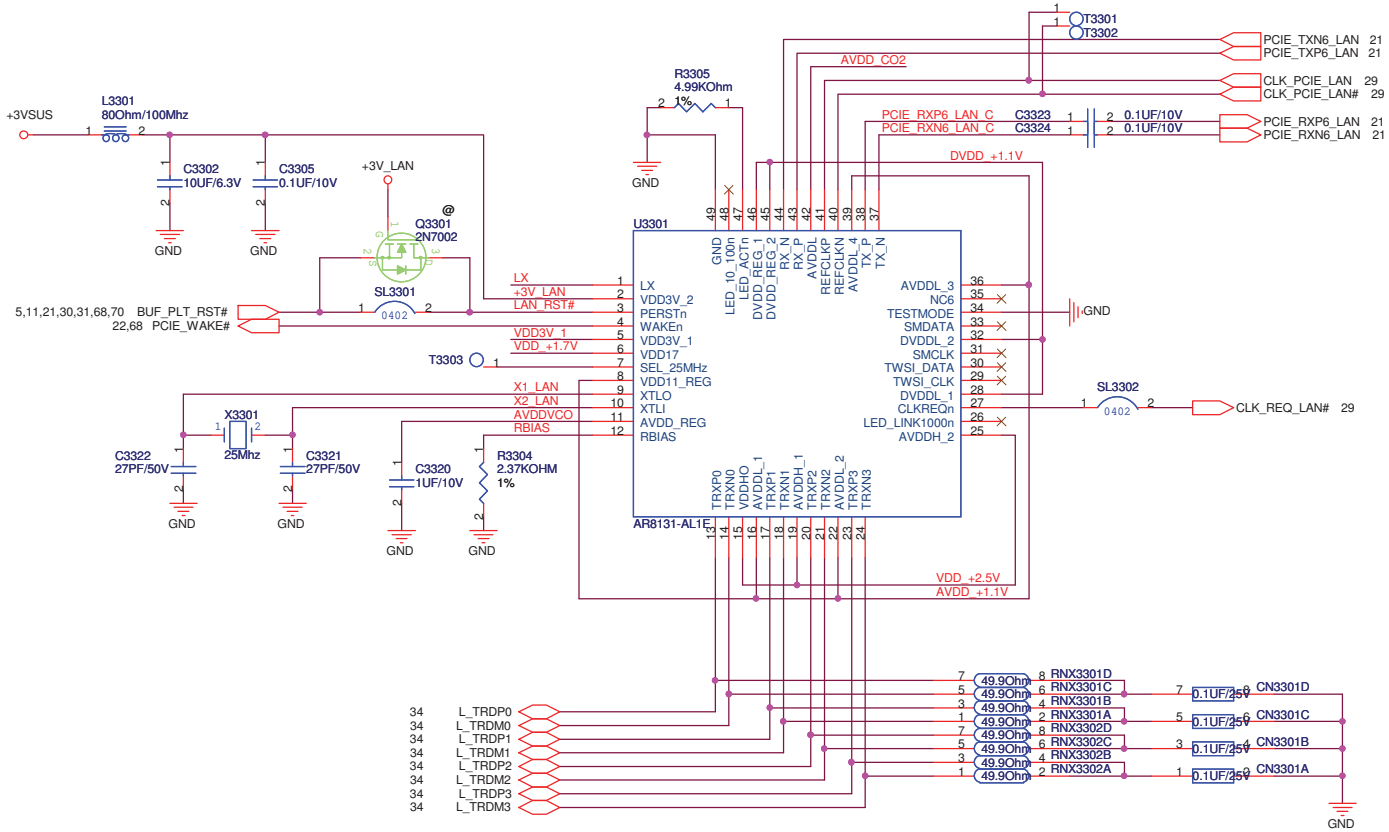
Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

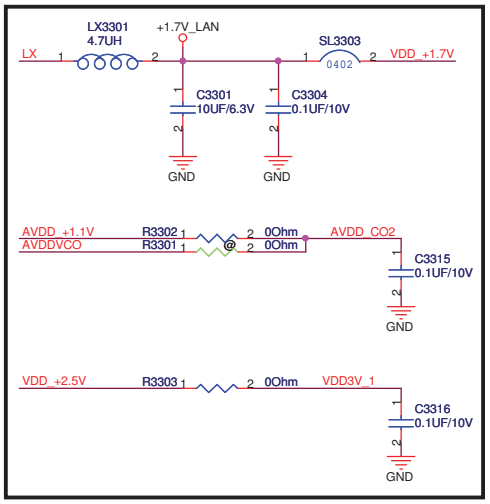
Date: Monday, April 06, 2009 Sheet 31 of 97

<Variant Name>

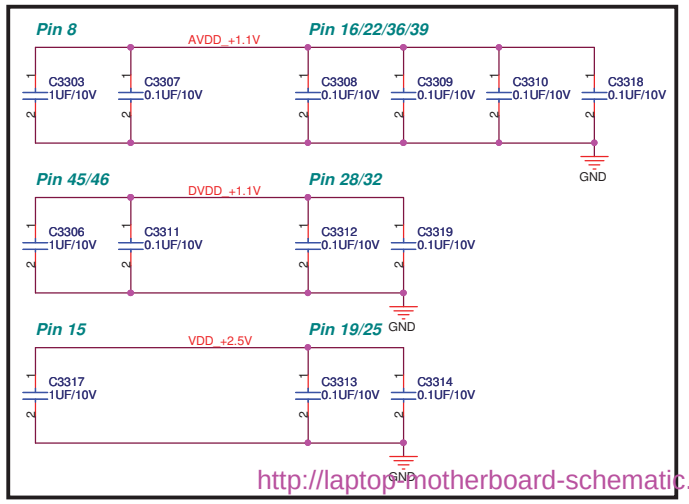
ASUSTeK COMPUTER INC	Title : UMA LEVEL SHIFTERS	
	Engineer: Tony Su	
Size: C	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 32 of 97	



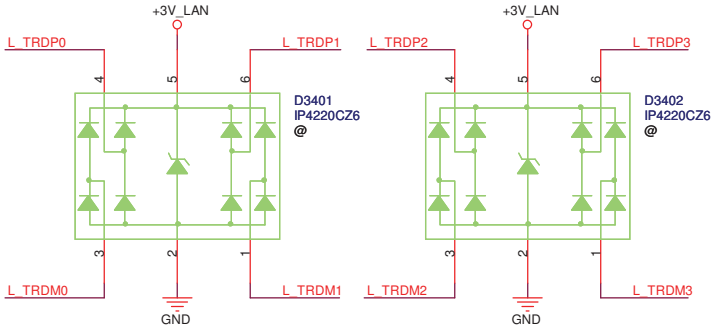
Power

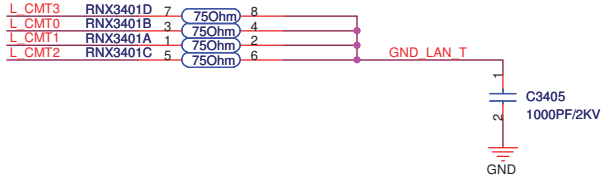


Cap.

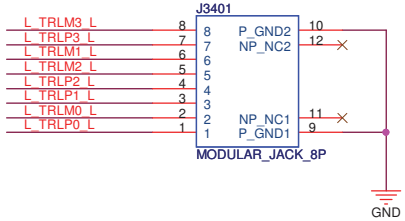


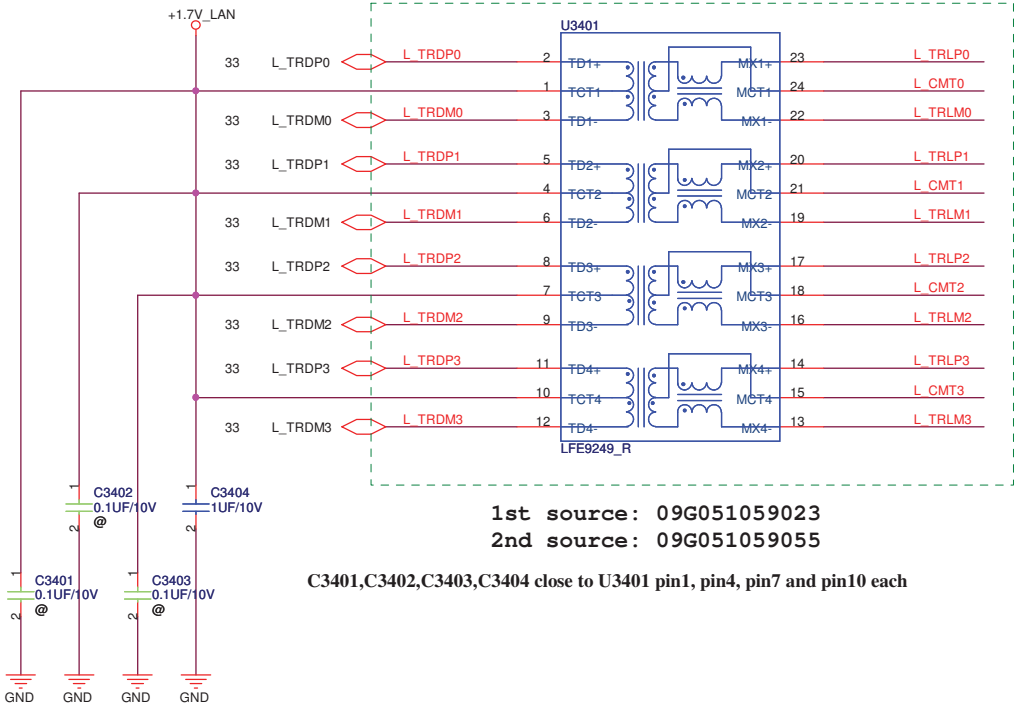
ASUSTeK COMPUTER INC. NB1	Title : LAN-AR8131-AR8121	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.00
Date: Wednesday, April 08, 2009	Sheet 33 of 97	





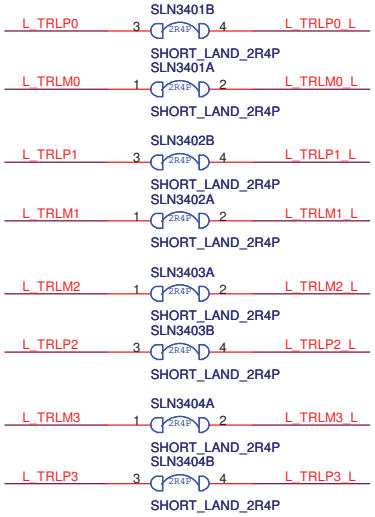
For RJ-45





1st source: 09G051059023
2nd source: 09G051059055

C3401,C3402,C3403,C3404 close to U3401 pin1, pin4, pin7 and pin10 each



<Variant Name>

Title : LAN RJ45 CONN

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0

Date: Tuesday, March 31, 2009 Sheet 34 of 97

<Variant Name>

Title : LAN RJ45 CONN

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0

Date: Tuesday, March 31, 2009 Sheet 35 of 97

<Variant Name>

Title : AUD ALC269

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 36 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 37 of 97

<Variant Name>

AUD HP&SPK&MIC&DMI CONN

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	U20A	1.0a

Date: Tuesday, March 31, 2009 Sheet 38 of 97

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: *Tony Su*	
Size: A	Project Name: **UX50**	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 39 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: *Tony Su*	
Size: A	Project Name: **UX50**	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 40 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: *Tony Su*	
Size: A	Project Name: **UX50**	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 41 of 97	

<Variant Name>

ASUSTeK COMPUTER INC

Title : CARD READER AU6371

Engineer: Tony Su

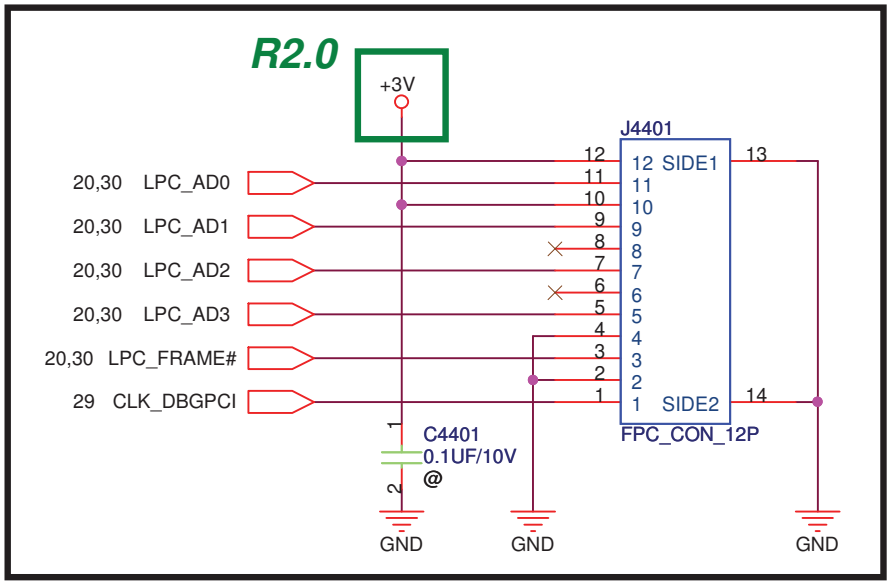
Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 42 of 97

<Variant Name>

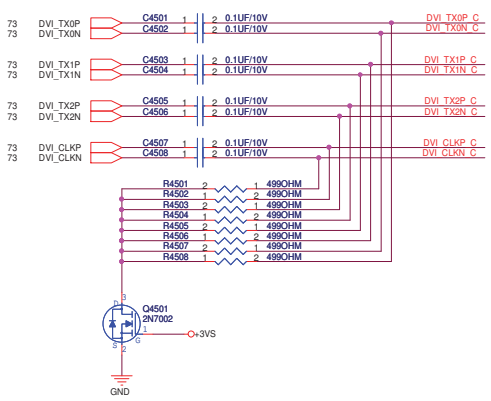
ASUSTeK COMPUTER INC	Title : CR EXPRESS CARD CONN	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 43 of 97	

LPC DEBUG PORT

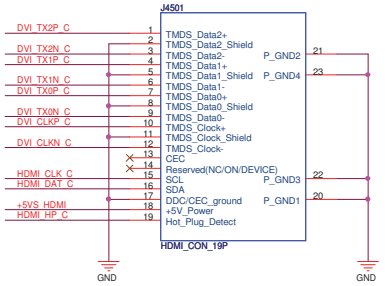


<Variant Name>

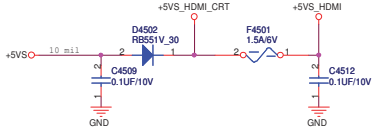
ASUSTeK COMPUTER INC	Title : BUG DEBUG PORT	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 44 of 97	

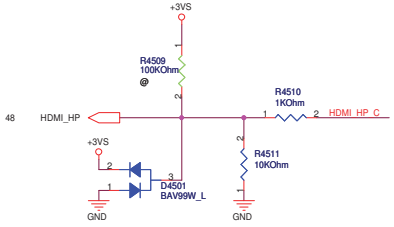


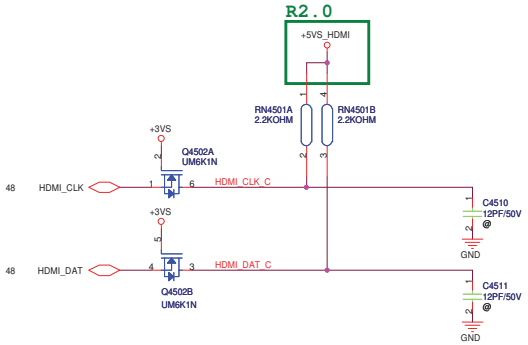
HDMI CON.



R2.0







<Variant Name>

ASUSTeK COMPUTER INC

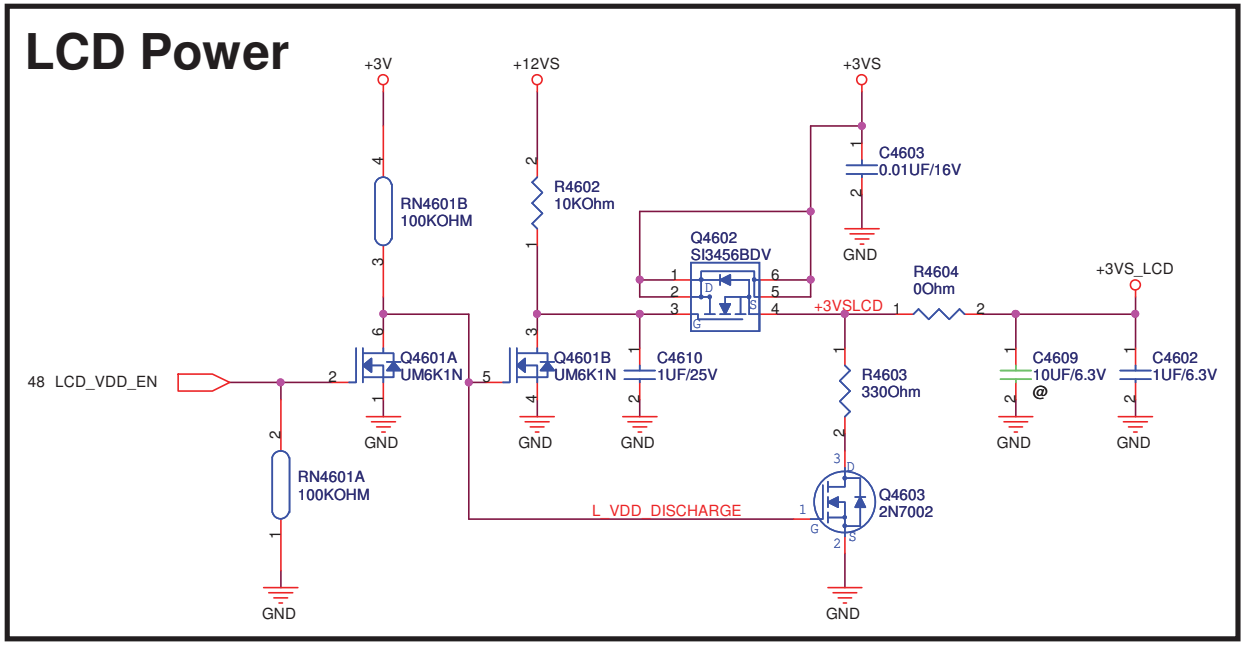
Title : HDMI CONN

Engineer: Tony Su

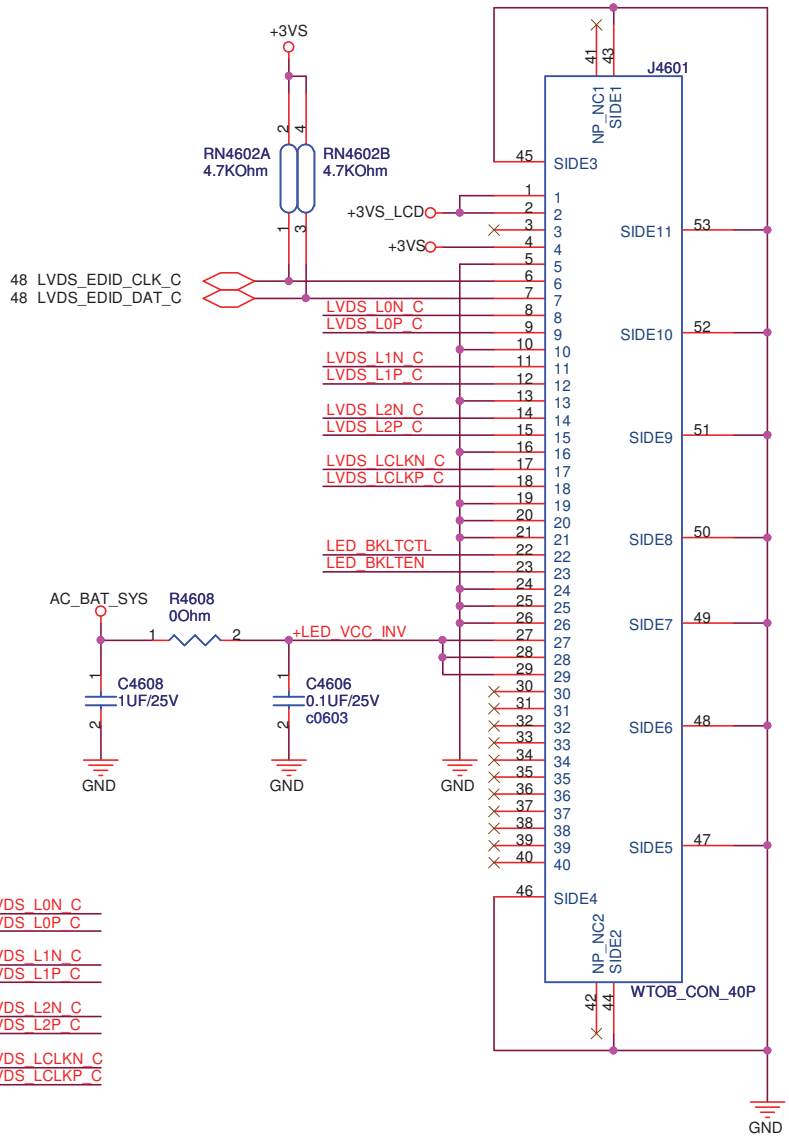
Size	Project Name	Rev
C	UX50	1.0a

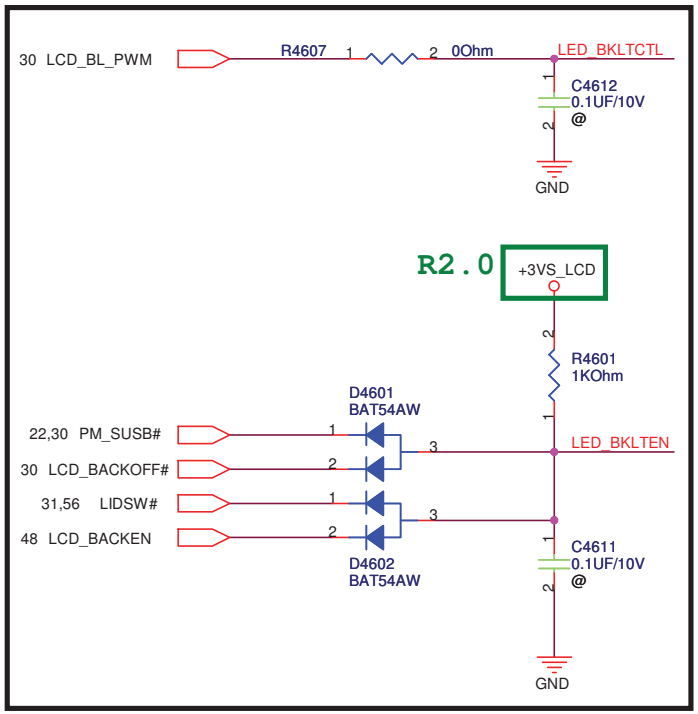
Date: Tuesday, March 31, 2009 Sheet 45 of 97

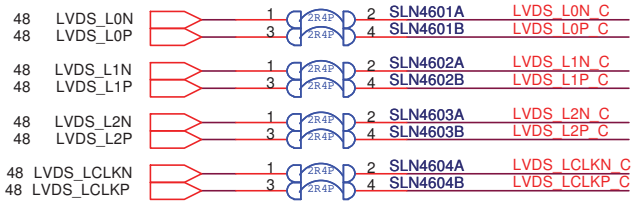
LCD Power



LVDS CONN







<Variant Name>

ASUSTeK COMPUTER INC

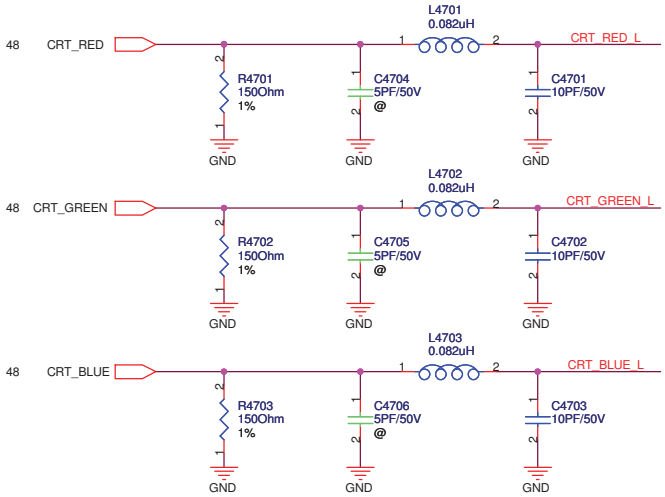
Title : CRT LVDS CONN

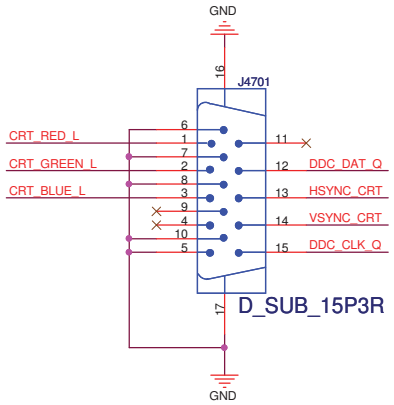
Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

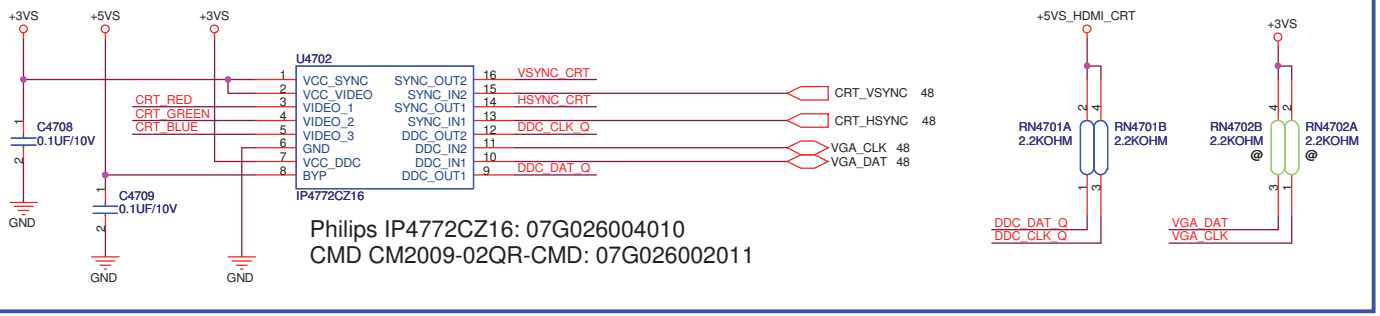
Date: Tuesday, March 31, 2009 Sheet 46 of 97

CRT Connector





PLACE ESD IC near J4701



<Variant Name>

ASUSTeK COMPUTER INC

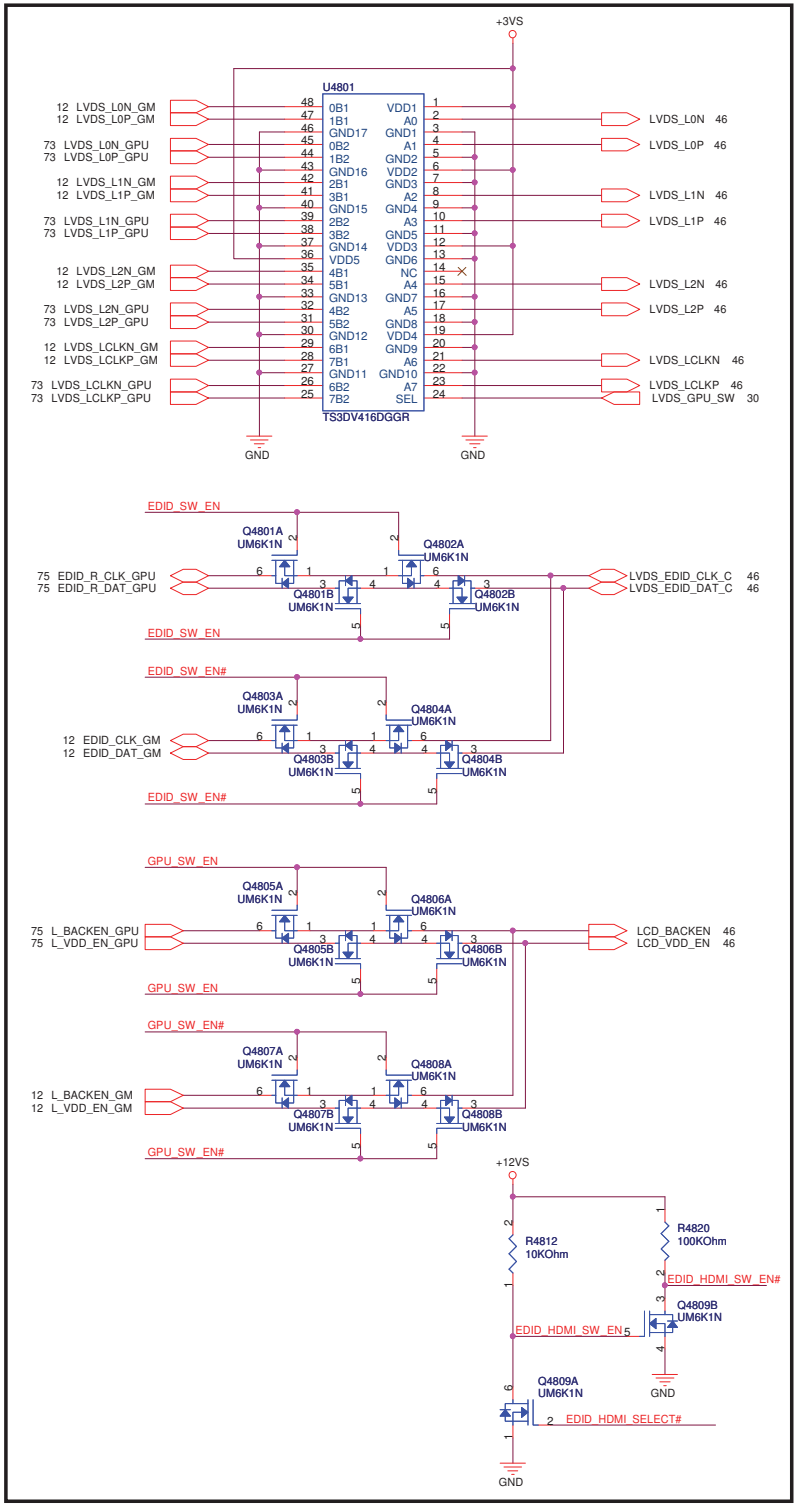
Title : CRT D-SUB CONN

Engineer: Tony Su

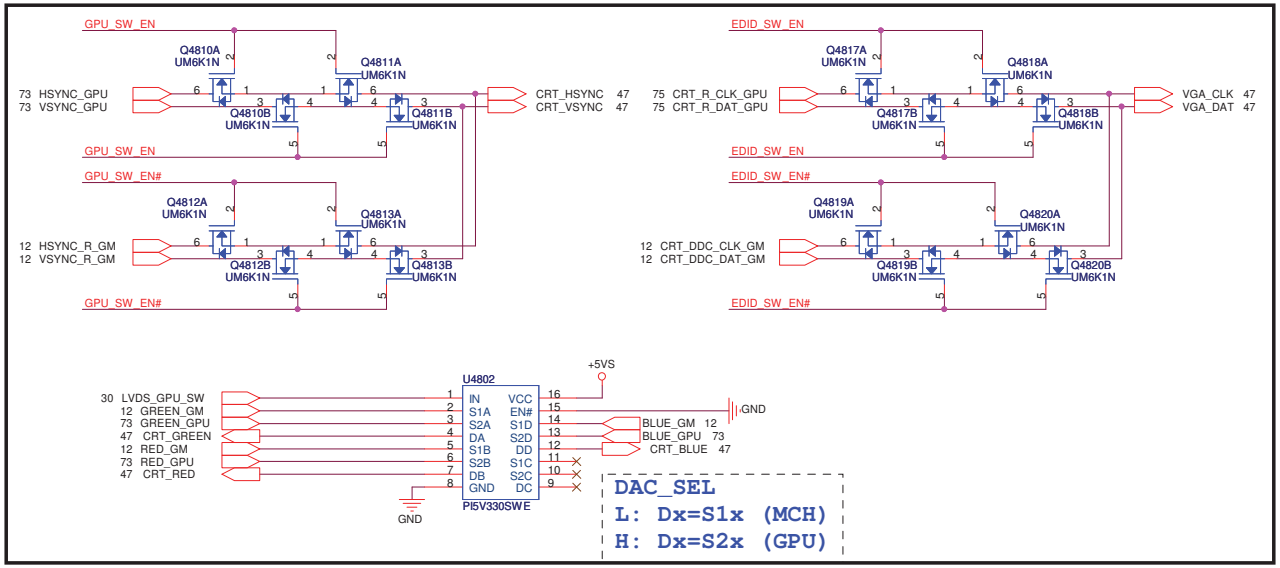
Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 47 of 97

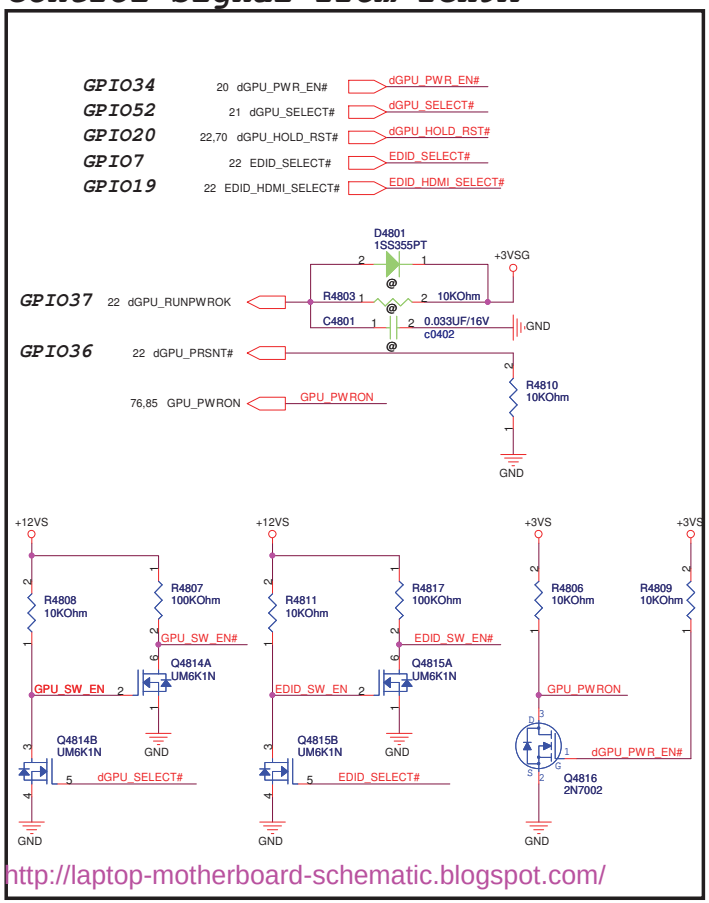
LVDS Switch



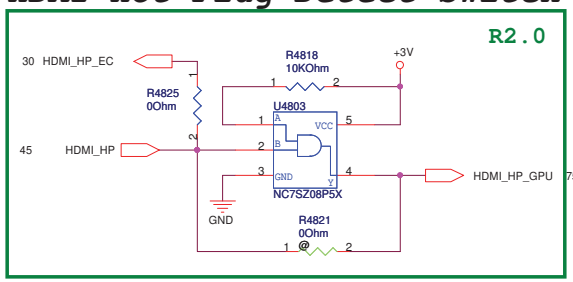
CRT Switch



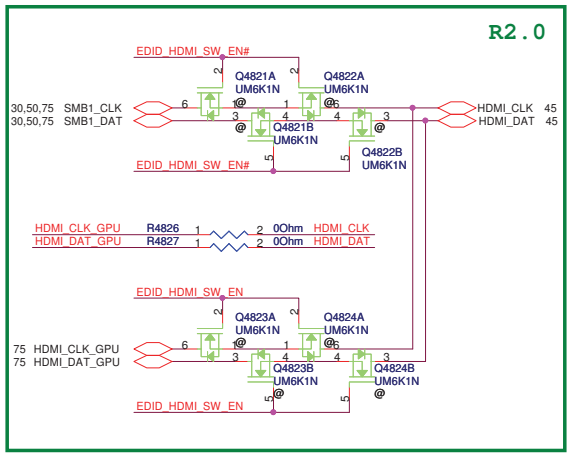
Control Signal from ICH9M



HDMI Hot-Plug Detect Switch



HDMI I2C Switch



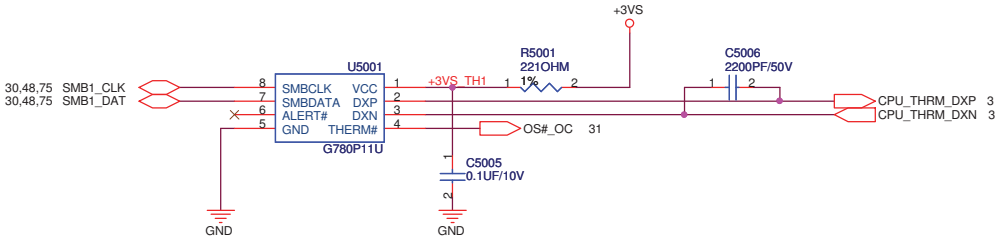
<Variant Name>

ASUSTeK COMPUTER INC	Title : Hybrid Switch	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 48 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT D-SUB CONN	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 49 of 97	

Thermal Seneor



1nd: 06G023096010 G780P11U SOP-8
2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

<Variant Name>

FAN THERMAL SENSOR FAN CONN

Title :

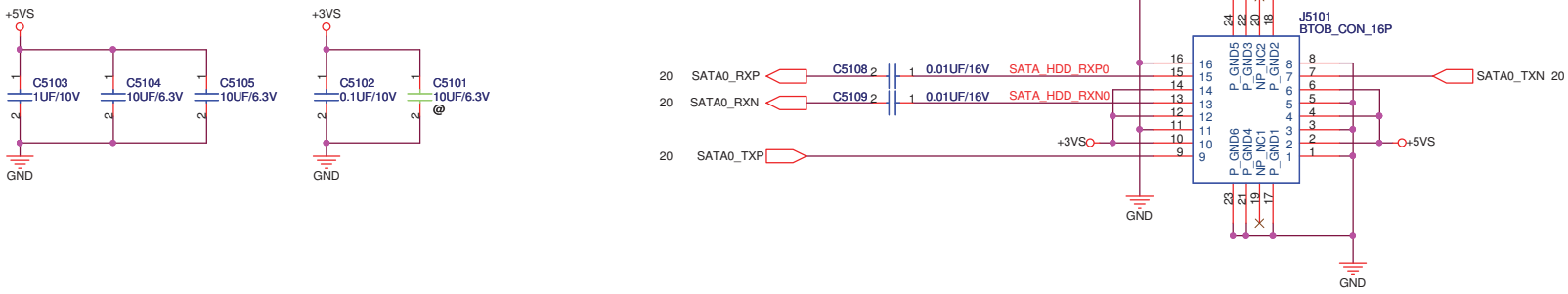
ASUSTeK COMPUTER INC

Engineer: Tony Su

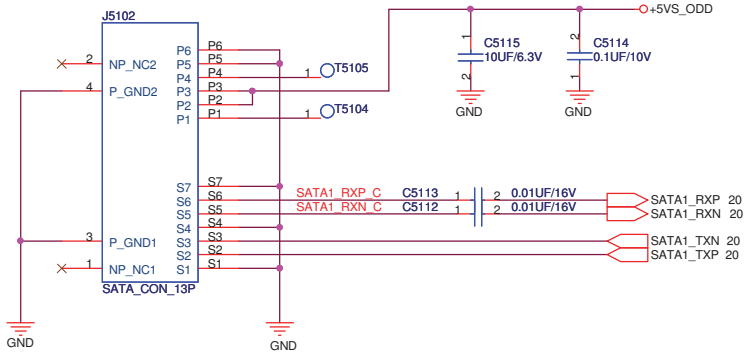
Size	Project Name	Rev
Custom	UX50	1.0a

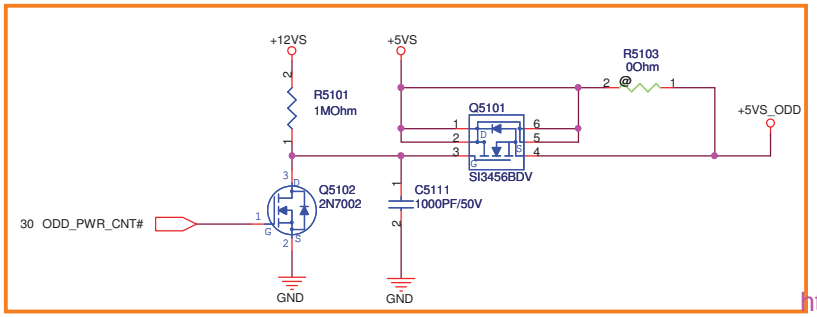
Date: Tuesday, March 31, 2009 Sheet 50 of 97

SATA HDD



SATA ODD





<Variant Name>

ASUSTeK COMPUTER INC	Title : XDD SATA HDD CONN	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 51 of 97	

<Variant Name>

Title : USB 2.0 CONN*1

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 52 of 97

ASUSTeK COMPUTER INC. NB1	Title : PCI_MiniCard		
	Engineer: Tony Su		
Size: Custom	Project Name: UX50		Rev: 1.00
Date: Tuesday, March 31, 2009	Sheet 53 of 97		

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 54 of 97

<Variant Name>

Title :

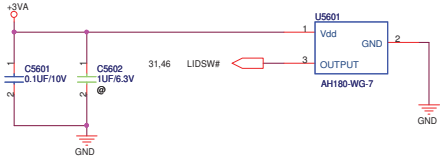
ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 55 of 97

LID SENSER



Hall Sensor Second Source
06G036012010 Cheap
06G036013010
06G036009011
06G051001012

<Variant Name>

LED PWR LED FOC CONN

Title :

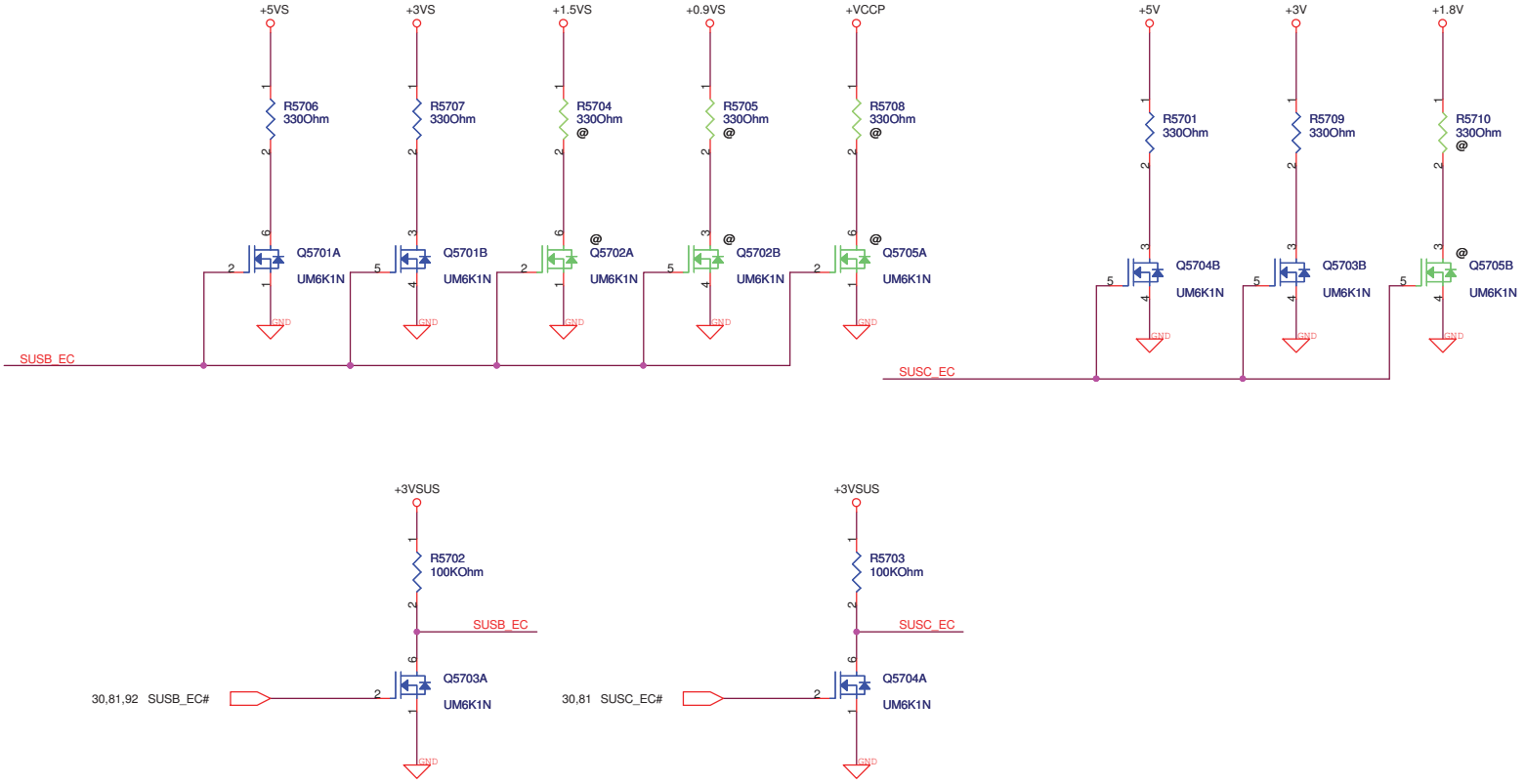
ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
C	UX50	1.0b

Date: Tuesday, March 31, 2009 Sheet 56 of 97

Discharge Circuit



<Variant Name>

ASUSTeK COMPUTER INC	Title : DSG DISCHARHE CIRCUIT	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 57 of 97	

<variant_name><Variant Name></variant_name>

Title :

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 58 of 97

<Variant Name>

Title :

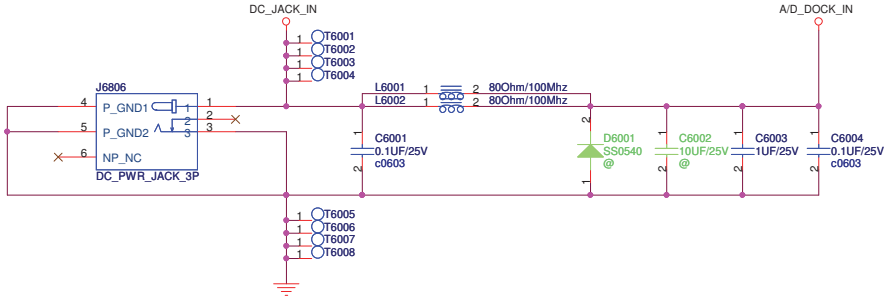
ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 59 of 97

DC IN



ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT IN	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.00
Date: Tuesday, March 31, 2009	Sheet 60 of 97	

<Variant Name>

ASUSTeK COMPUTER INC	Title : BT BLUETOOTH CONN	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 61 of 97	

<Variant Name>

Title : TPM

ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 62 of 97

<variant_name><Variant Name></variant_name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 63 of 97	

<Variant Name>

Title :

ASUSTeK COMPUTER INC

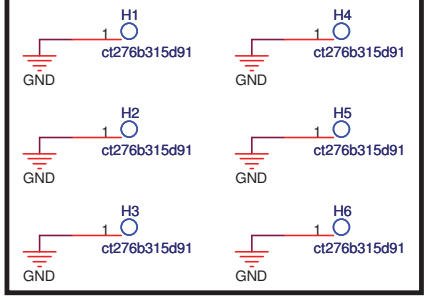
Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

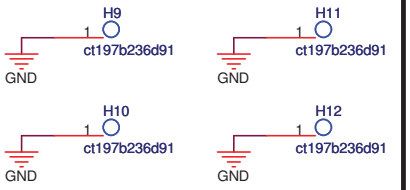
Date: Tuesday, March 31, 2009 Sheet 64 of 97

Screw Hole & SMT Nut

Boss

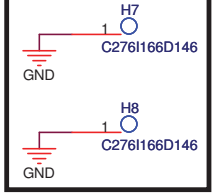


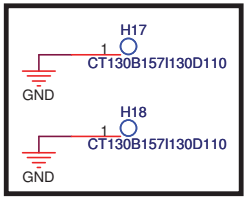
B to B



CPU

NB





<Variant Name>

ASUSTeK COMPUTER INC

ME SCREW HOLE AMT NUT

Title :

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 65 of 97

<Variant Name>

Title :

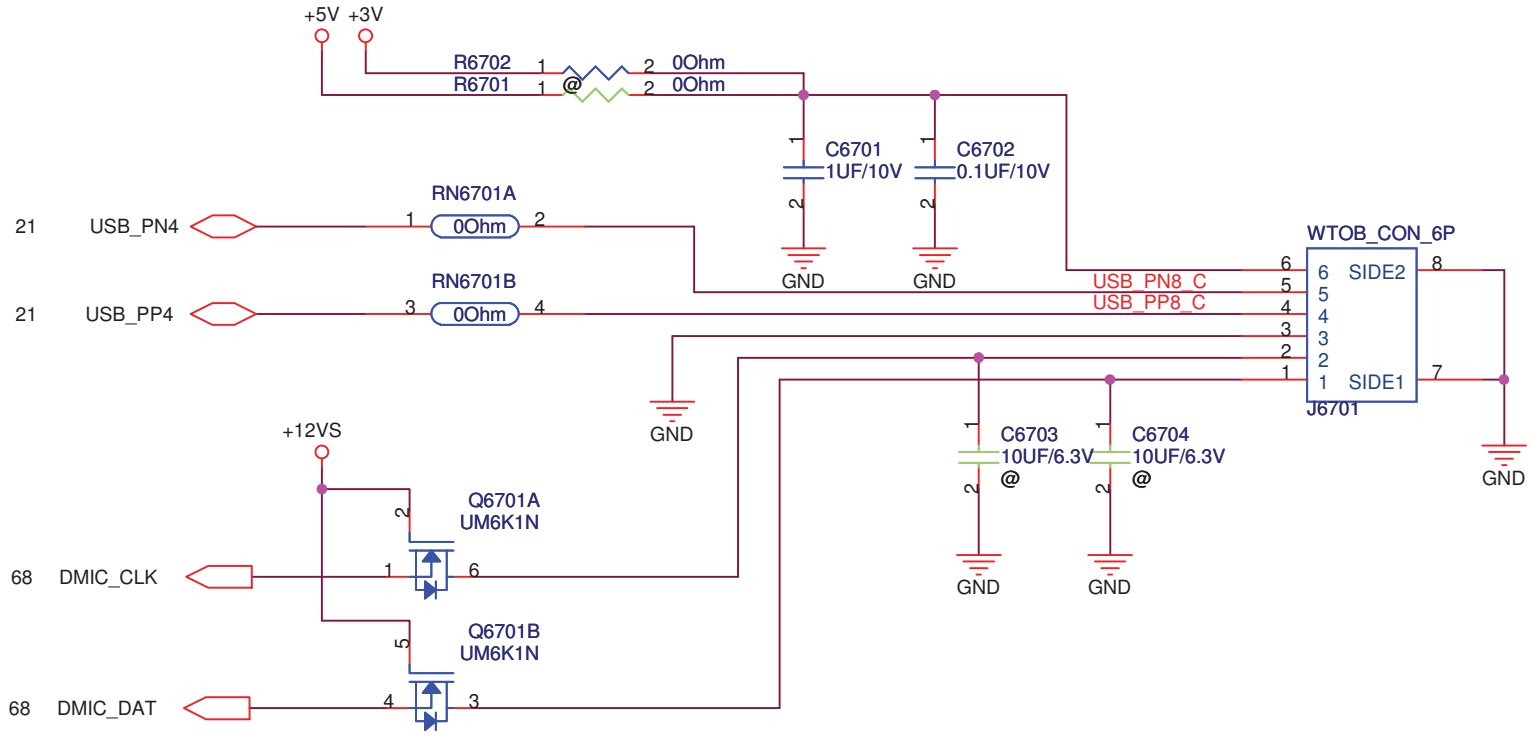
ASUSTeK COMPUTER INC

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 66 of 97

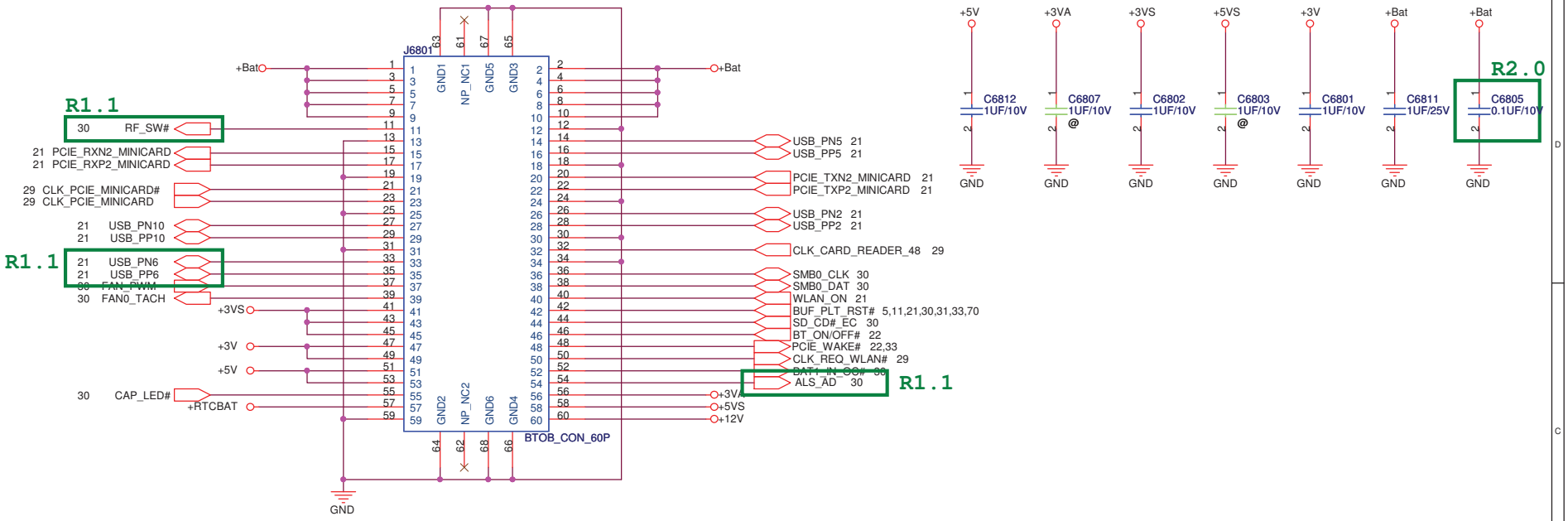
Camera Module



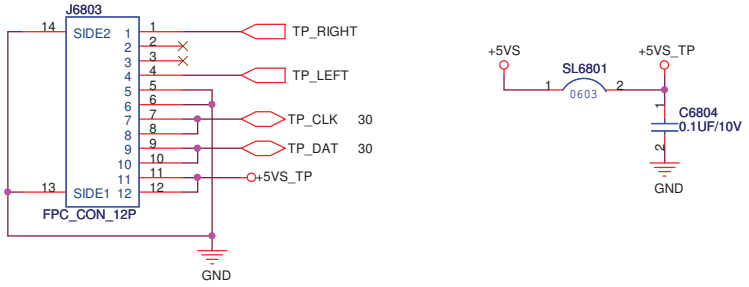
<Variant Name>

ASUSTeK COMPUTER INC	Title : CMOS CAMERA	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 67 of 97	

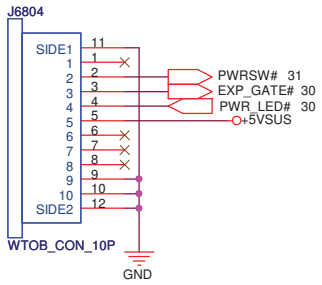
CR Board



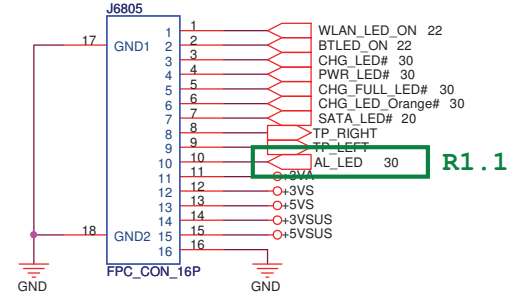
Touch Pad Board



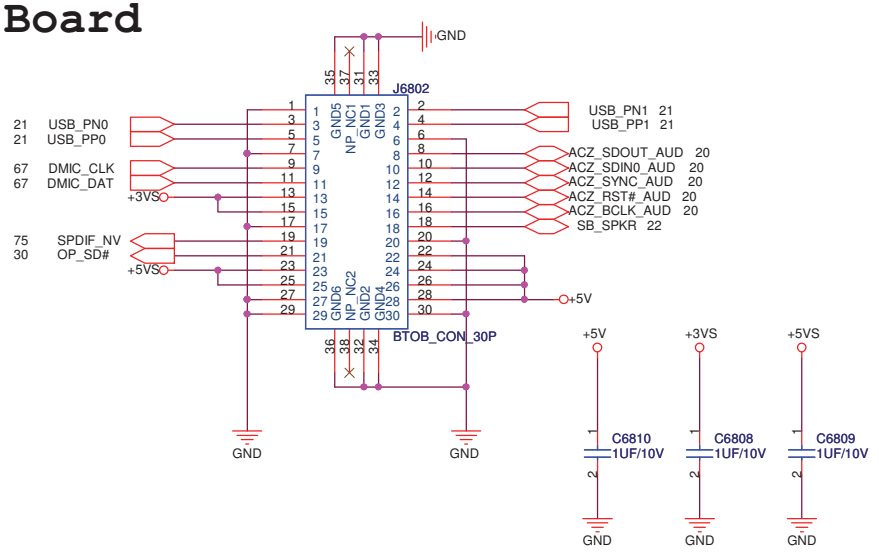
Switch Board



LED Board



Audio Board



<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN	
	Engineer: Tony Su	
Size: B	Project Name: UX50	Rev: 1.0a
Date: Tuesday, March 31, 2009	Sheet 68 of 97	

SYSTEM

+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,76,82
+VCC_GMCH	+VCC_GMCH	14
+VGFX_CORE	+VGFX_CORE	14
+3VS	+3VS	7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92
+VCORE	+VCORE	4,5,80
+1.5VS	+1.5VS	4,15,20,23,57,84
+5V	+5V	31,57,67,68,91
+5VS	+5VS	23,45,47,48,51,57,68,80,84,91
+3VA	+3VA	20,30,31,56,68,81,88
+VCC_RTC	+VCC_RTC	20,23
+3V	+3V	44,46,48,57,67,68,70,91
+3VSUS	+3VSUS	20,21,22,23,30,33,57,68,76,81,85,91,92
+5VSUS	+5VSUS	23,68,80,81,82,83,85,86,88,91
+3VPLL	+3VPLL	30
+3VACC	+3VACC	30
+3VA_EC	+3VA_EC	30,31
+12V	+12V	68,91
+12VS	+12VS	22,46,48,51,67,91
AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85,86,88
+5VA	+5VA	81

<Variant Name>

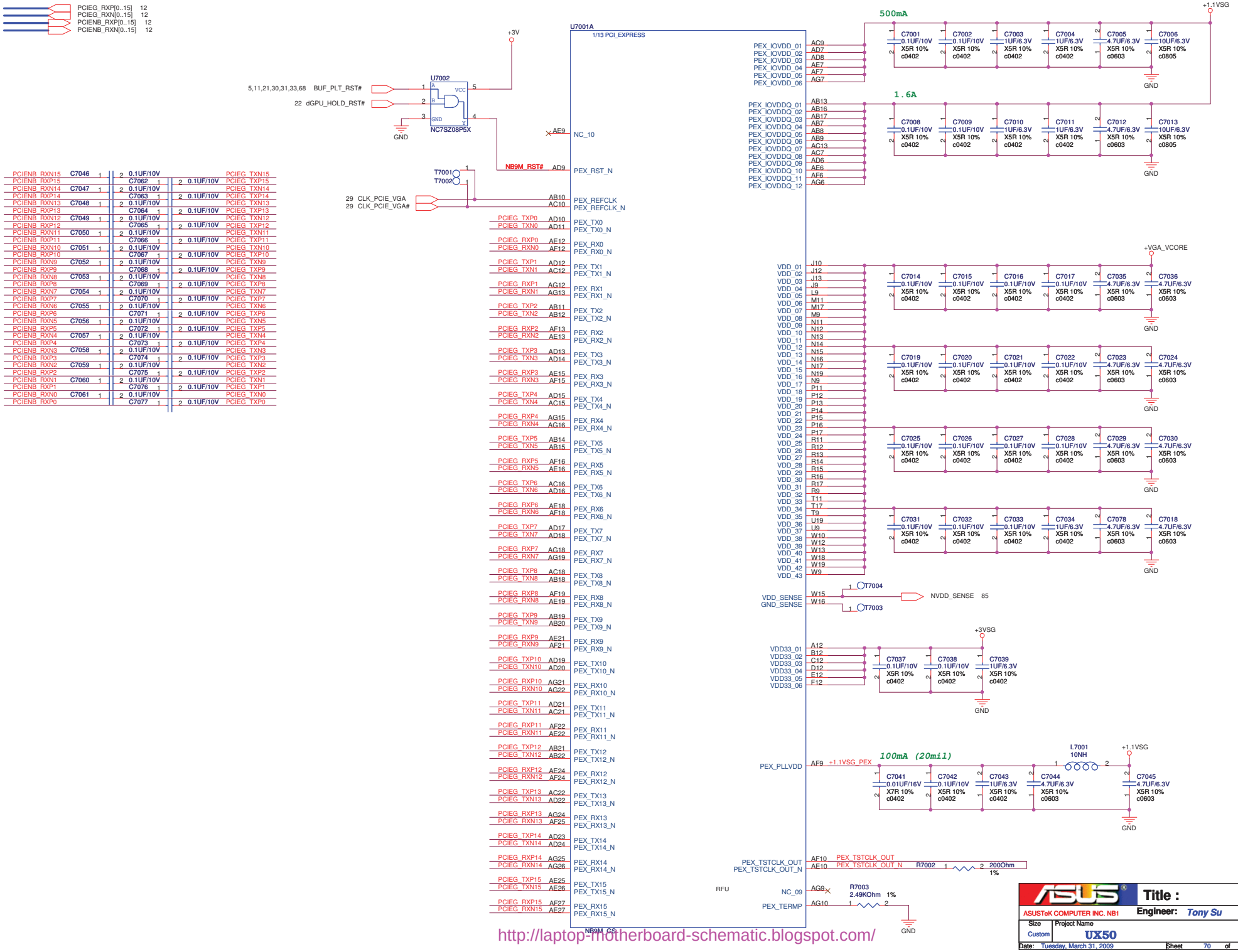
ASUSTeK COMPUTER INC

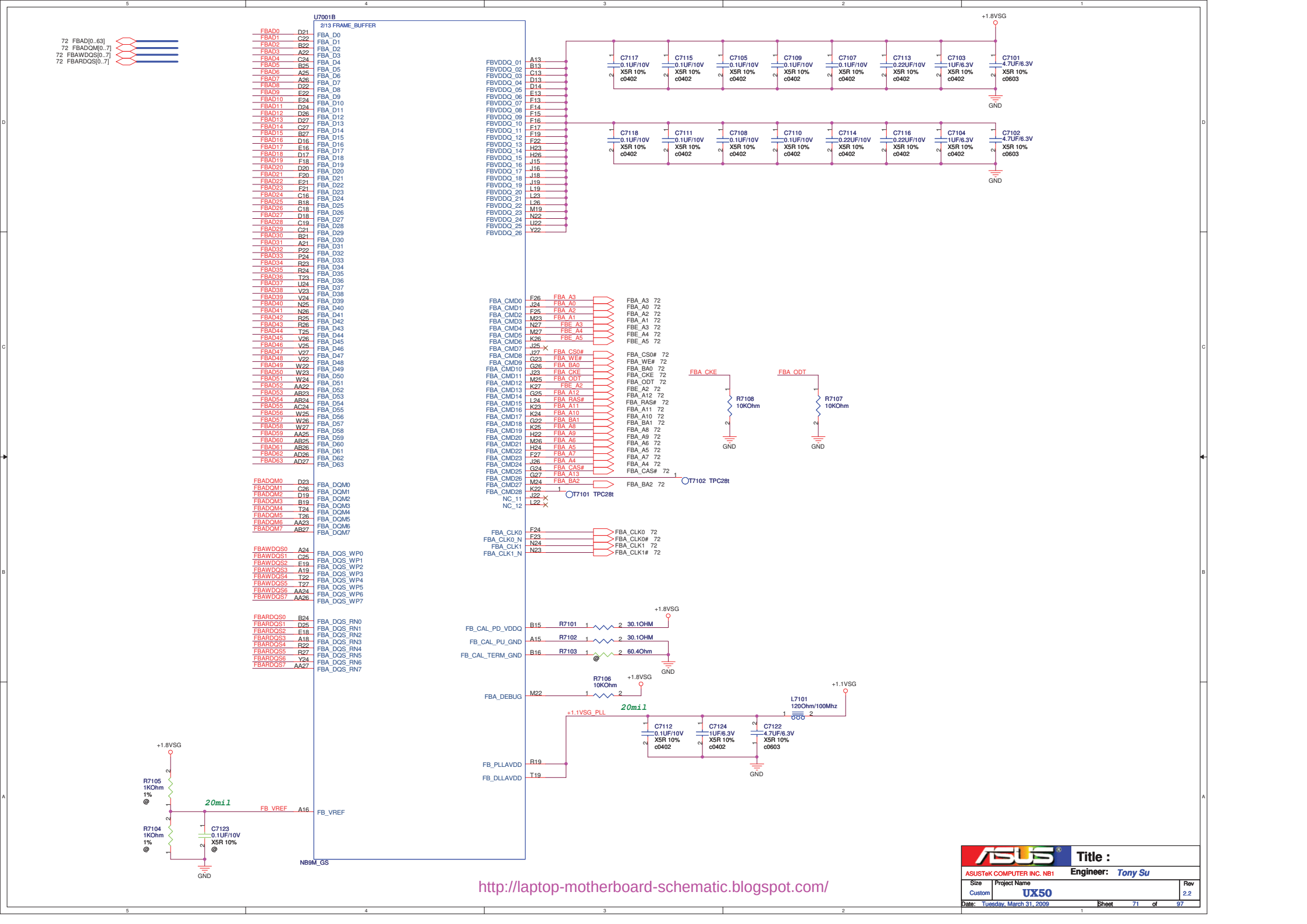
Title :

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 69 of 97





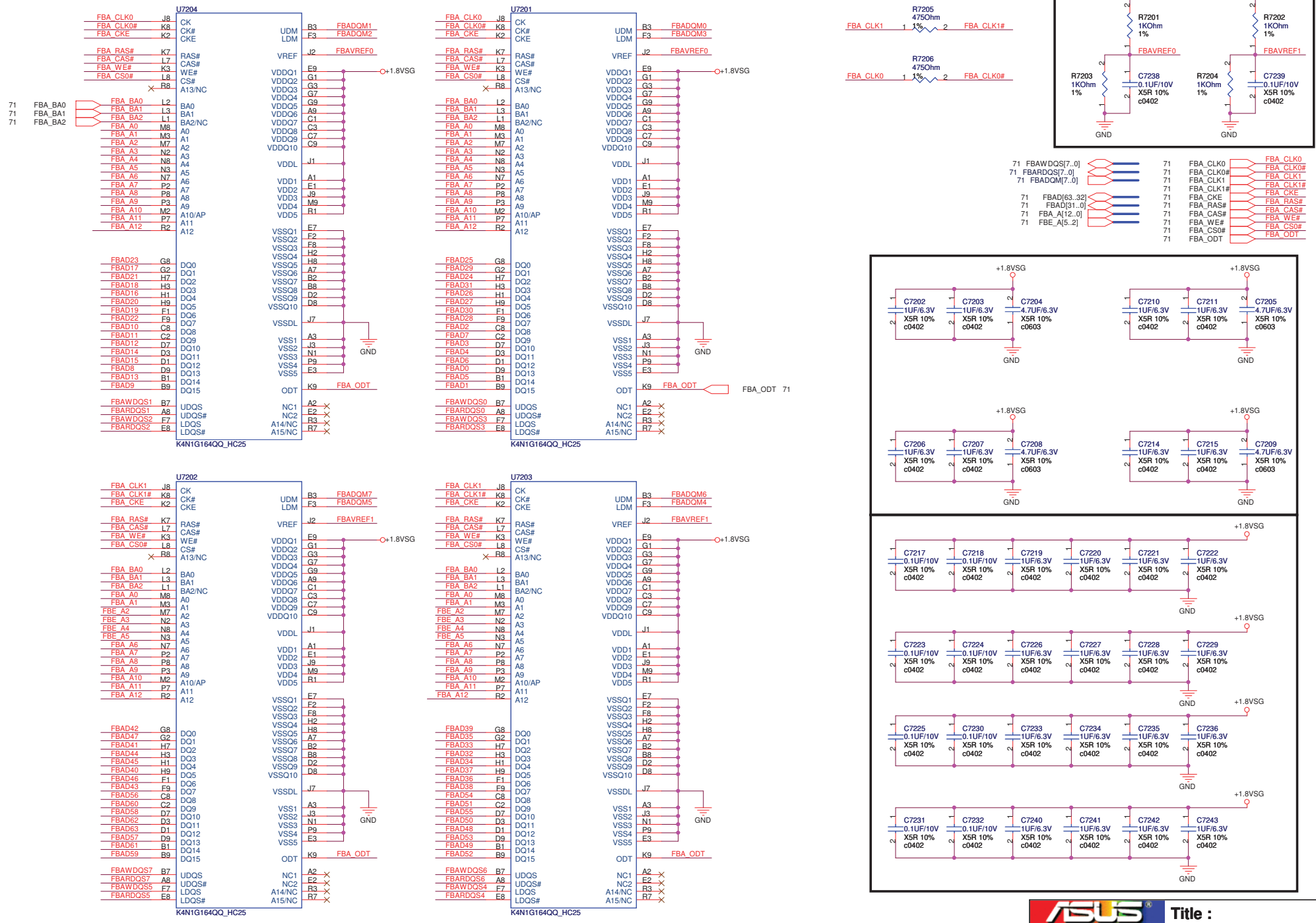
ASUSTeK COMPUTER INC. NB1

Title :

Engineer: Tony Su

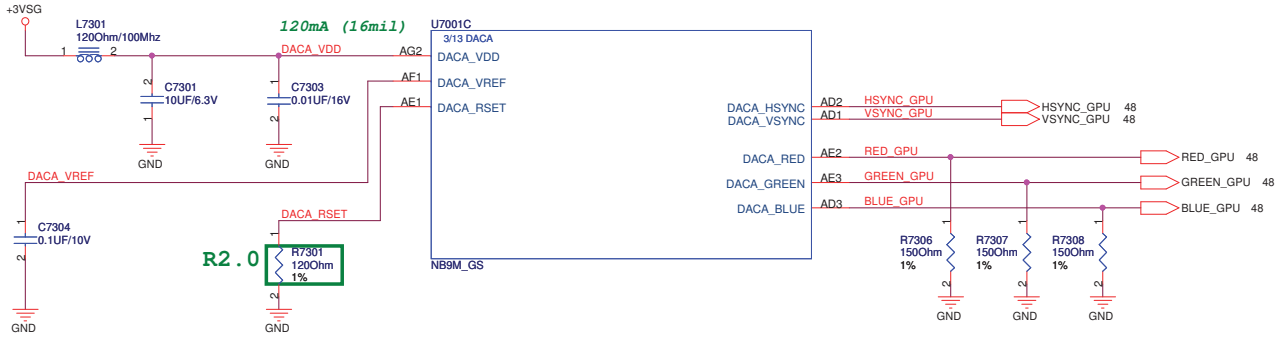
Size	Project Name	Rev
Custom	UX50	2.2

Date: Tuesday, March 31, 2009 Sheet 71 of 97

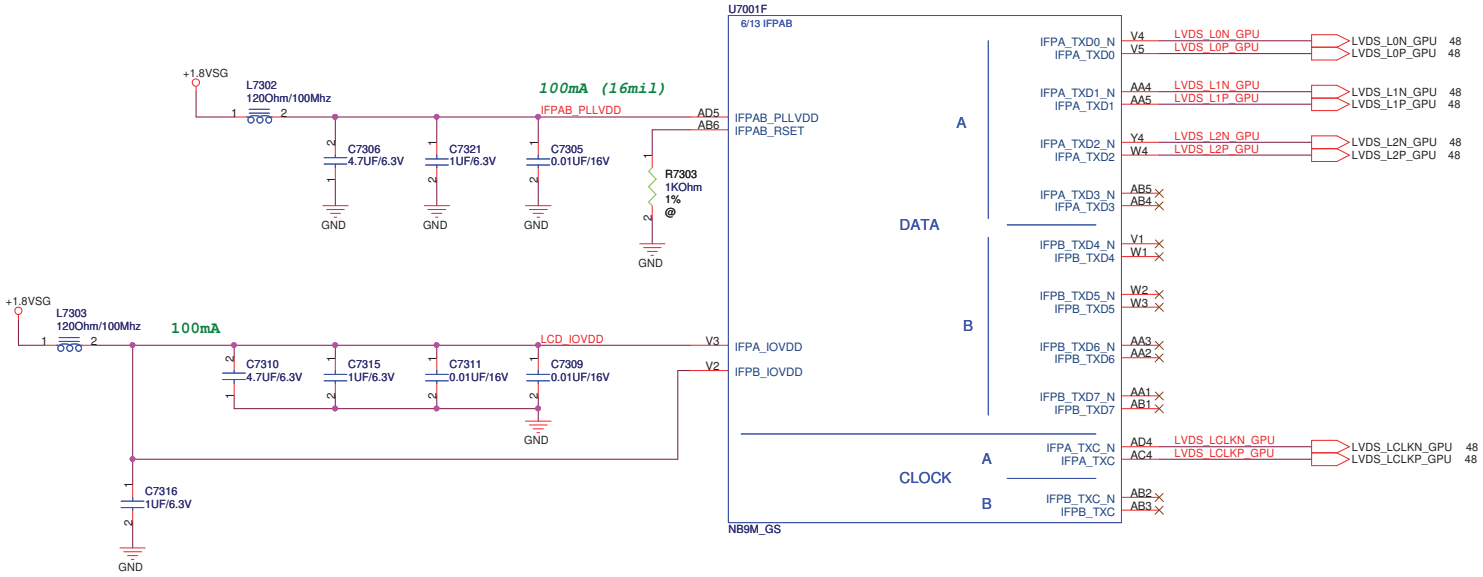


ASUSTeK COMPUTER INC. NB1	Engineer: Tony Su		
Size: Custom	Project Name: UX50		Rev: 2.2
Date: Monday, April 06, 2009	Sheet 72 of 97		

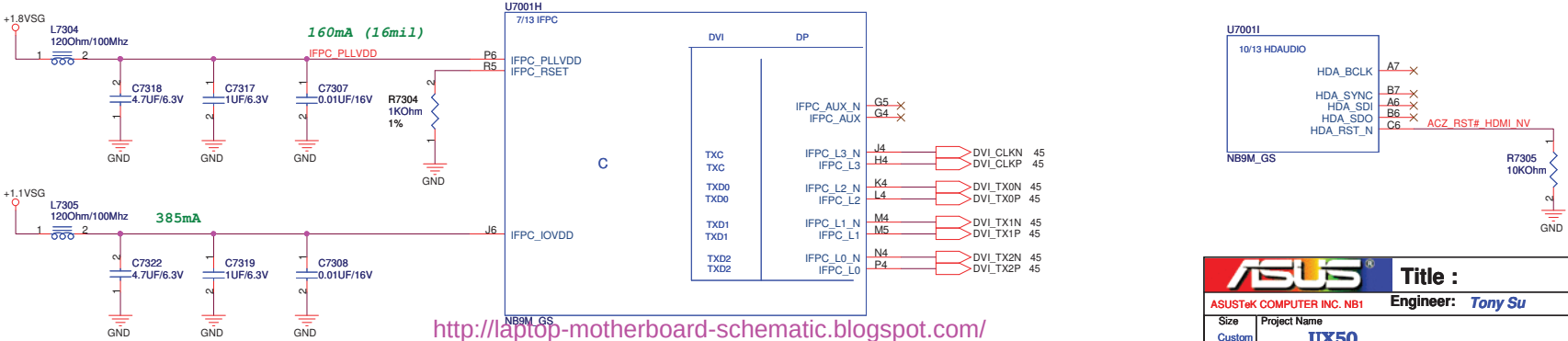
VGA



LVDS

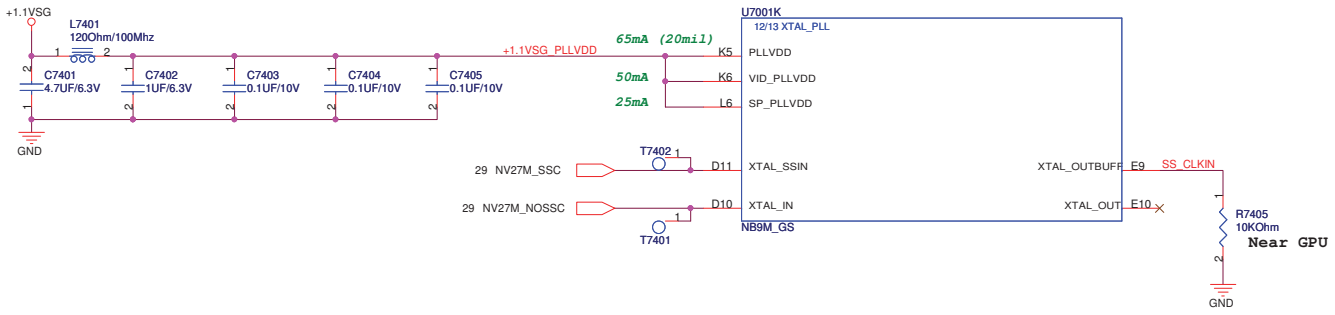


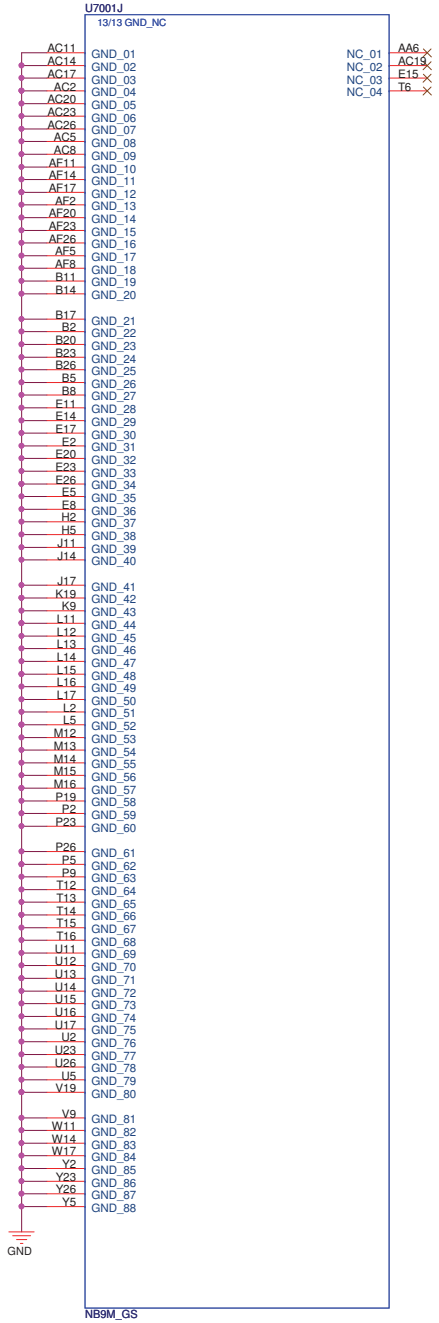
HDMI



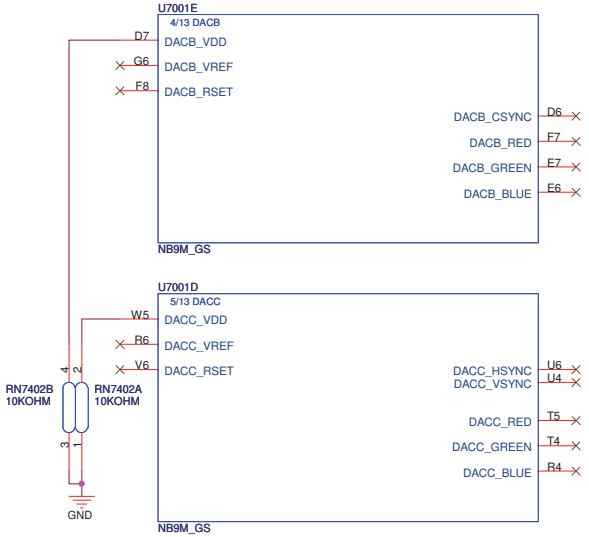
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 2.2
Date: Tuesday, March 31, 2009	Sheet 73 of 97	

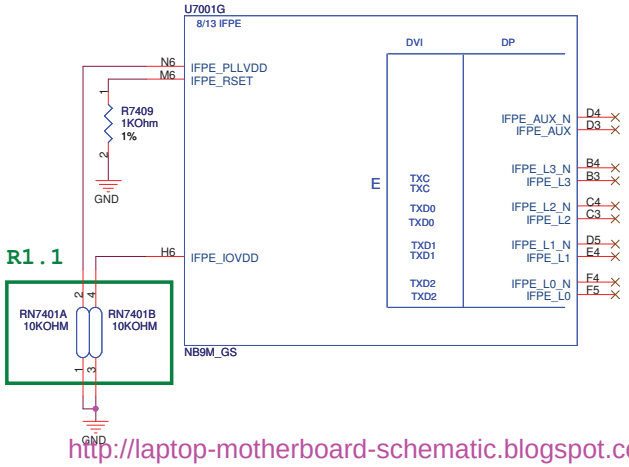
Xtal





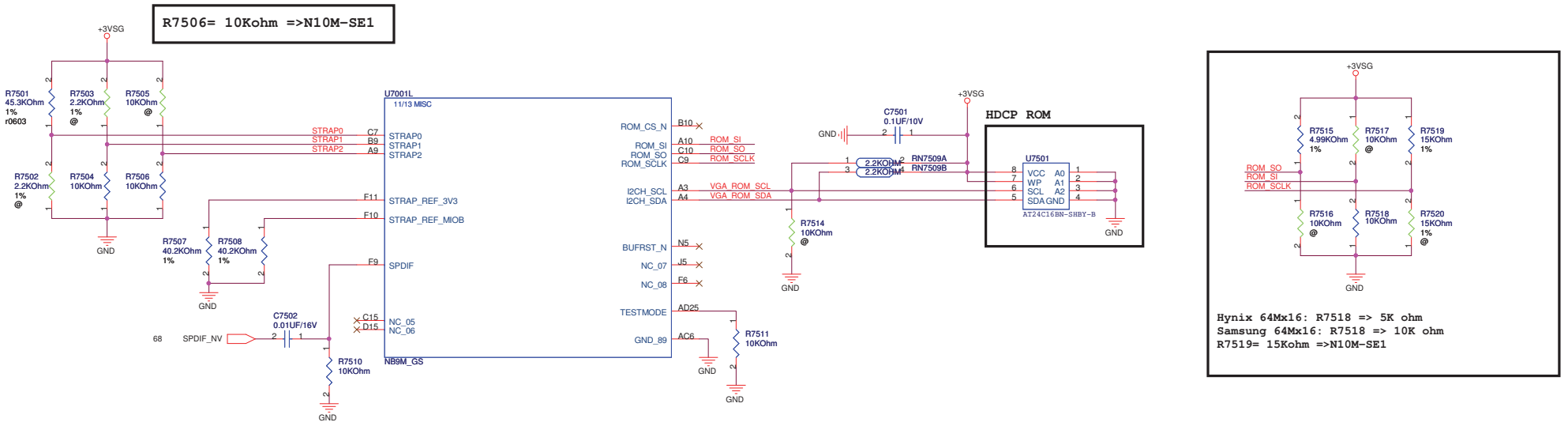
Other





ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: Tony Su		
Size: Custom	Project Name: UX50		Rev: 2.2
Date: Tuesday, March 31, 2009	Sheet 74 of 97		

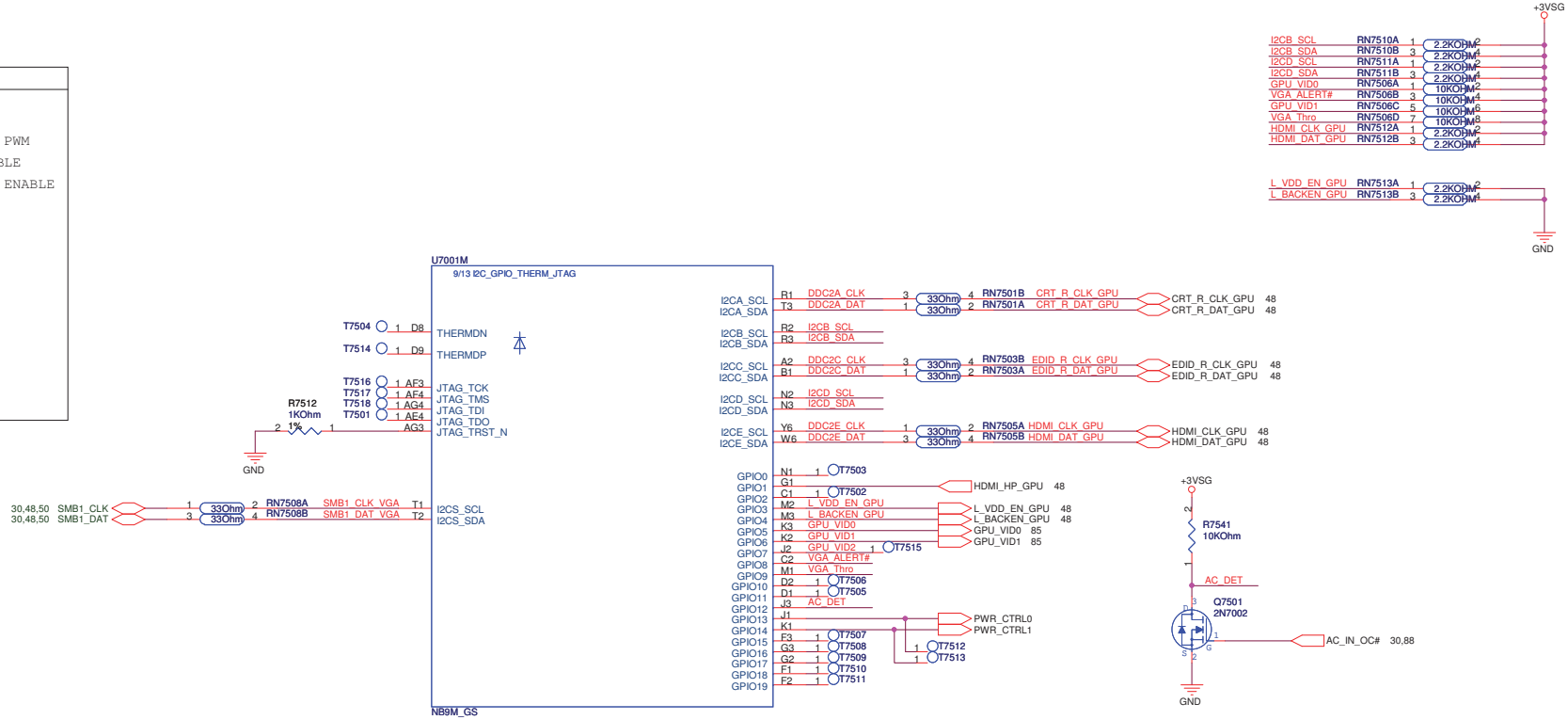
ROM



GPIO

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL



ASUSTeK COMPUTER INC. NB1 Engineer: Tony Su

Title :

Size	Project Name	Rev
Custom	UX50	2.2

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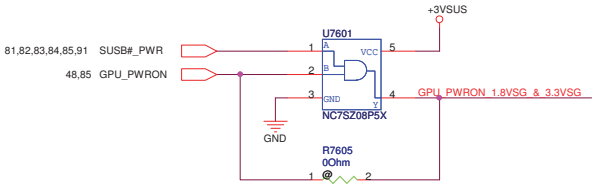
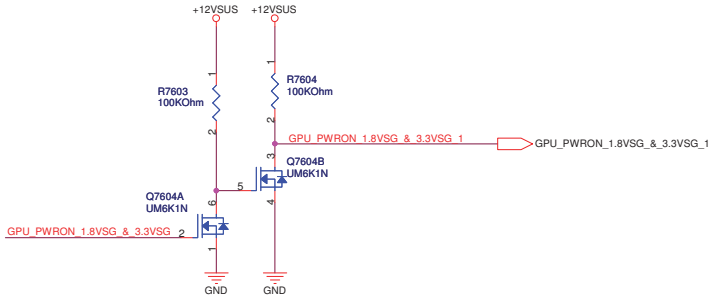
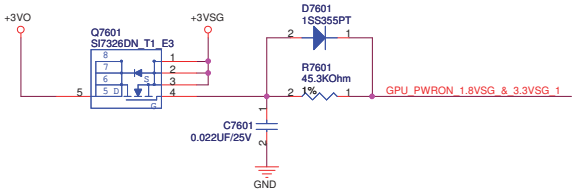
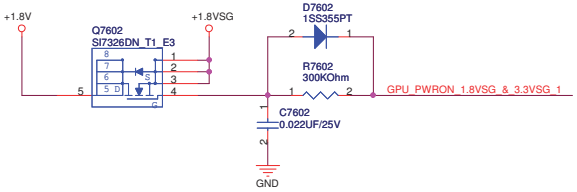
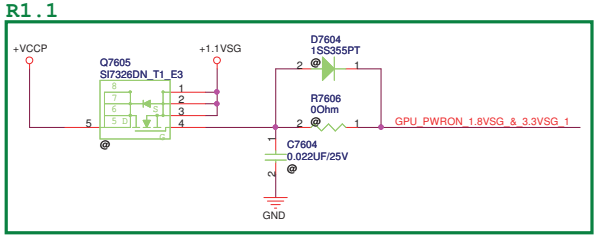








R1.1

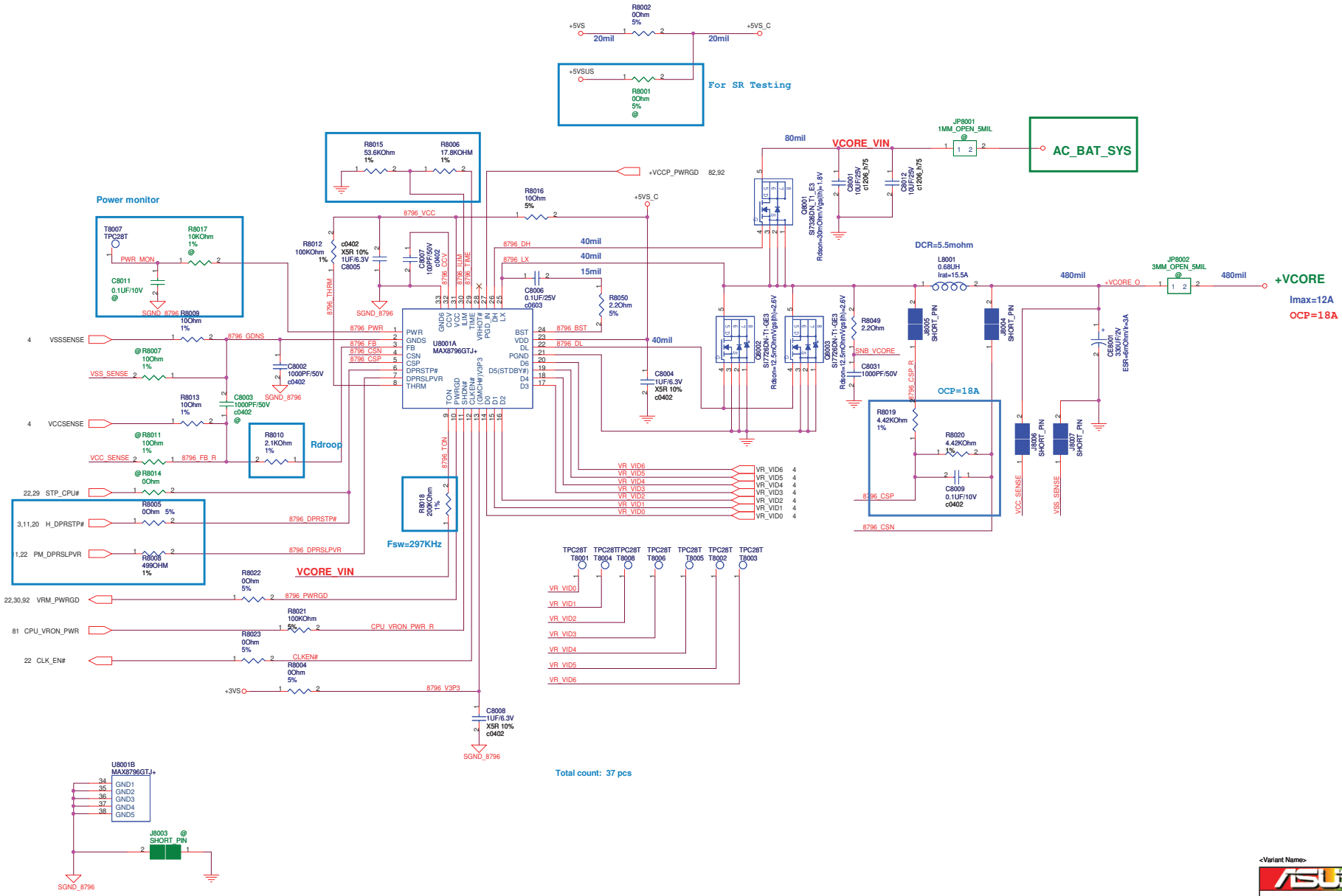


ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: Custom	Project Name: UX50	Rev: 2.2
Date: Wednesday, April 01, 2009	Sheet 76 of 97	

Title :	Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1	Engineer: Tony Su
Size: A	Project Name: UX50
Rev: 2.2	
Date: Tuesday, March 31, 2009	Sheet 77 of 97

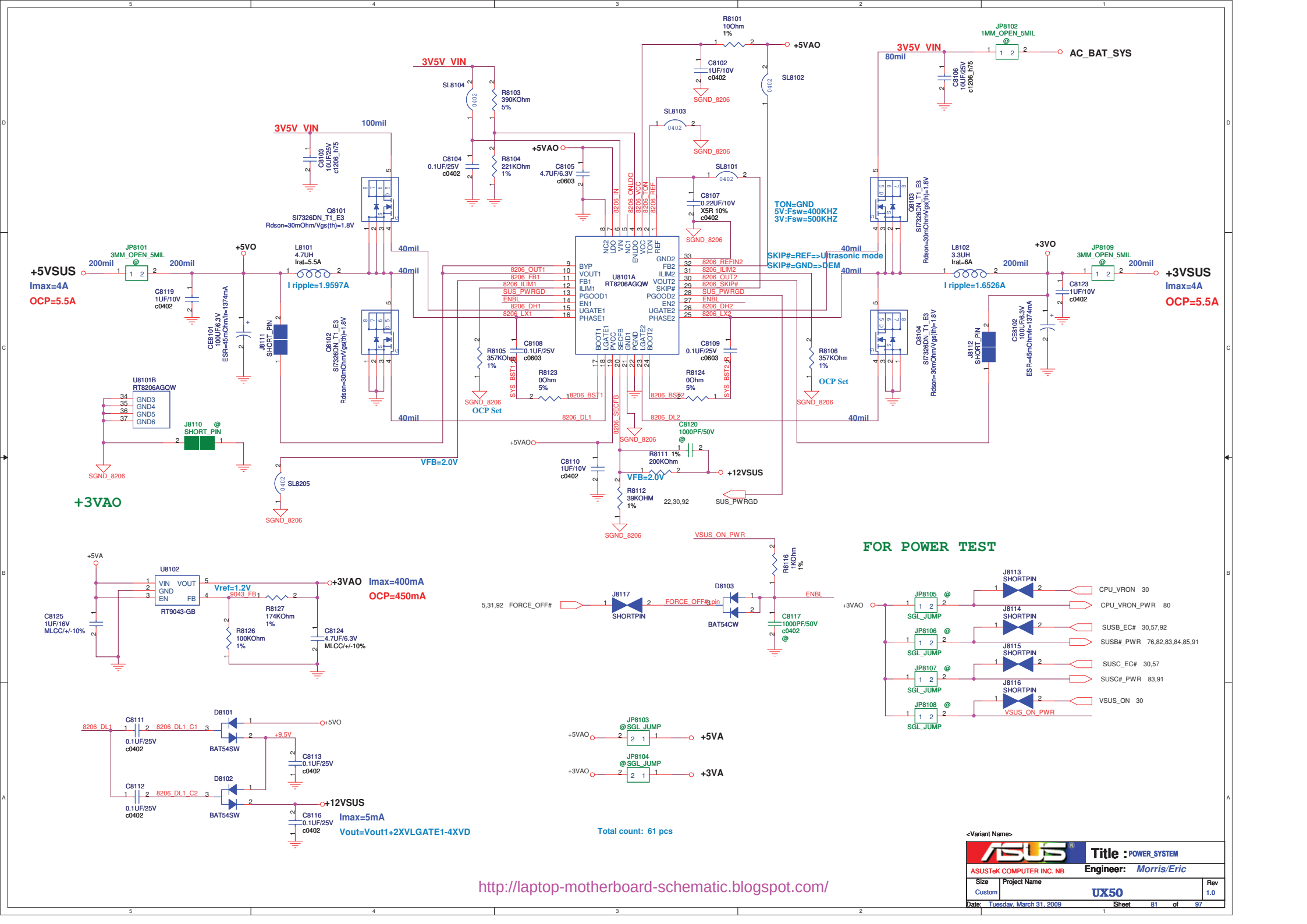
ASUSTeK COMPUTER INC. NB1		Title : Cantiga-POWER(5)	
		Engineer: Tony Su	
Size: A	Project Name: UX50		Rev: 2.2
Date: Tuesday, March 31, 2009		Sheet 78 of 97	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Tony Su	
Size: A	Project Name: UX50	Rev: 2.2
Date: Tuesday, March 31, 2009	Sheet 79 of 97	



<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : +VCORE	
	Engineer: Morris/Eric	
Size: Custom	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 80 of 97	


+5VSUS
Imax=4A
OCP=5.5A
+3VSUS
Imax=4A
OCP=5.5A
+3VAO
Imax=400mA
OCP=450mA
+12VSUS
Imax=5mA
Vout=Vout1+2XVLGATE1-4XVD
AC_BAT_SYS
3V5V_VIN
80mil
100mil
200mil
40mil
I ripple=1.9597A
I ripple=1.6526A
TON=GND
5V:Fsw=400KHZ
3V:Fsw=500KHZ
SKIP#=REF=>Ultrasonic mode
SKIP#=GND=>DEM
OCP Set
VFB=2.0V
Vref=1.2V
U8101A
RT8206AGQW
U8101B
RT8206AGQW
U8102
RT9043-GB
Q8101
SI7326DN_T1_E3
Rdson=30mOhm/Vgs(th)=1.8V
Q8102
SI7326DN_T1_E3
Rdson=30mOhm/Vgs(th)=1.8V
Q8103
SI7326DN_T1_E3
Rdson=30mOhm/Vgs(th)=1.8V
Q8104
SI7326DN_T1_E3
Rdson=30mOhm/Vgs(th)=1.8V
FOR POWER TEST
CPU_VRON 30
CPU_VRON_PWR 80
SUSB_EC# 30,57,92
SUSB#_PWR 76,82,83,84,85,91
SUSC_EC# 30,57
SUSC#_PWR 83,91
VSUS_ON 30
Total count: 61 pcs
http://laptop-motherboard-schematic.blogspot.com/
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Morris/Eric
Project Name
UX50
Rev 1.0
Date: Tuesday, March 31, 2009
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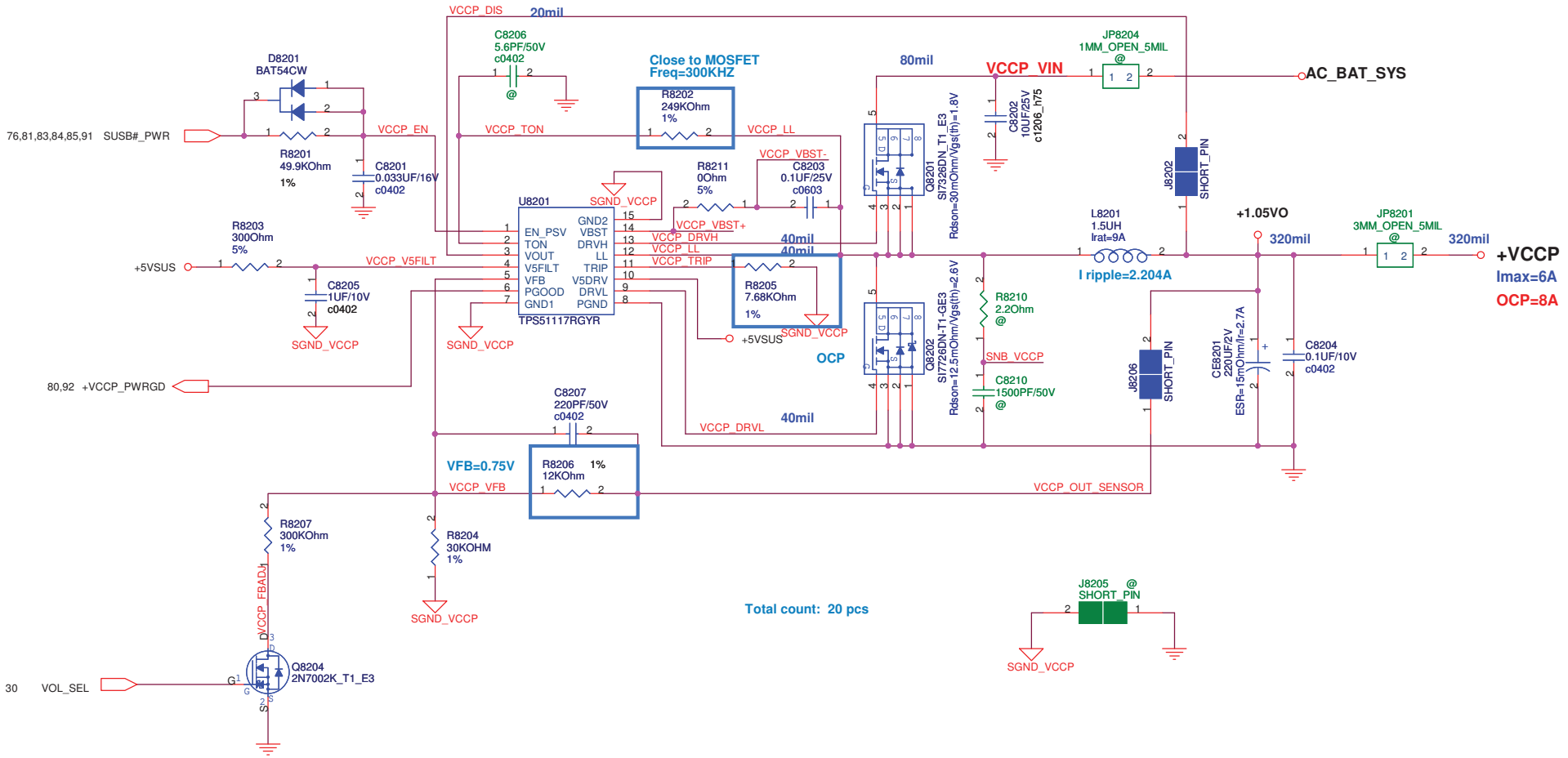


<Variant Name>

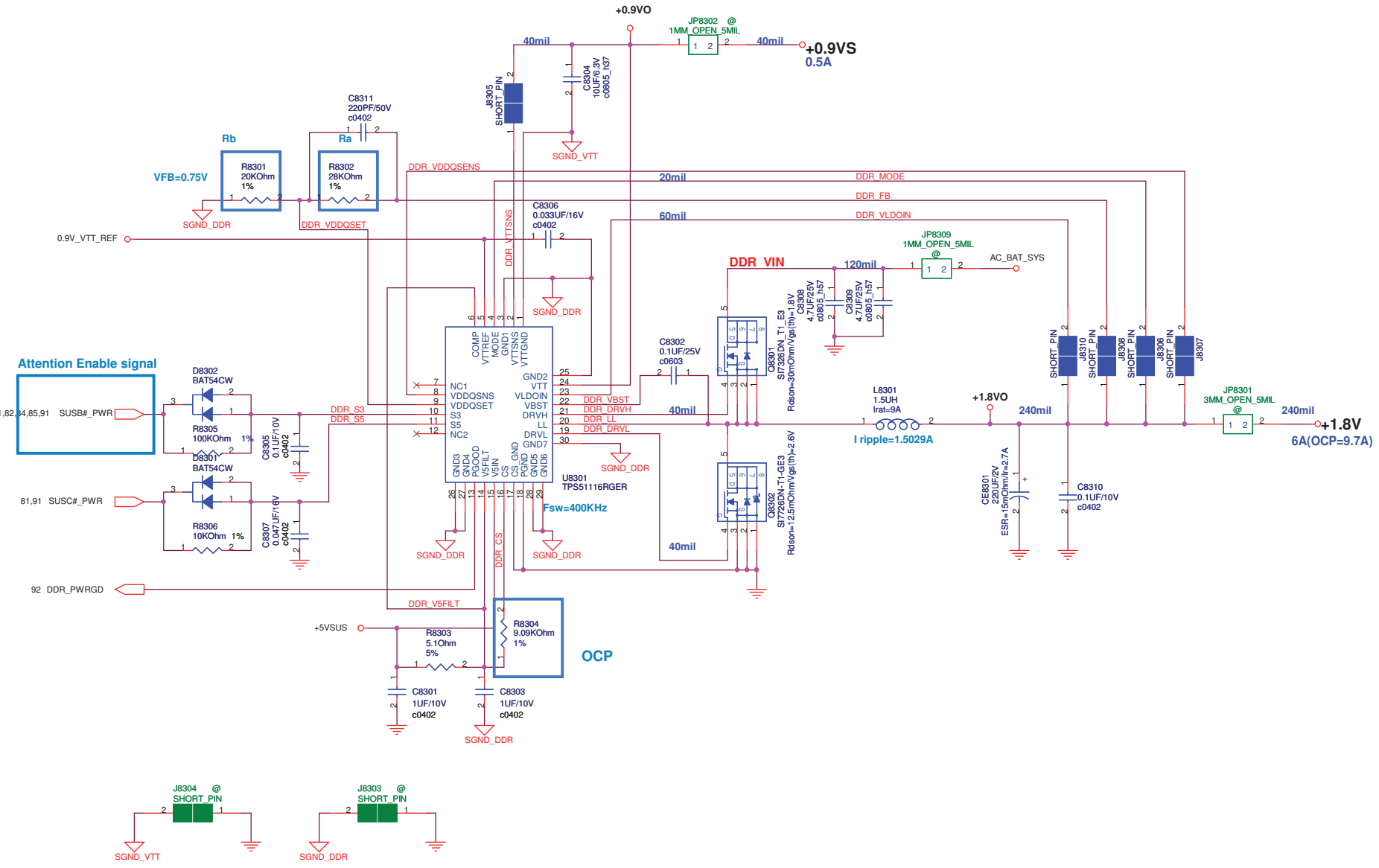
ASUSTeK COMPUTER INC. NB

Title :POWER_I/O_+VCCP

Engineer: Morris/Eric

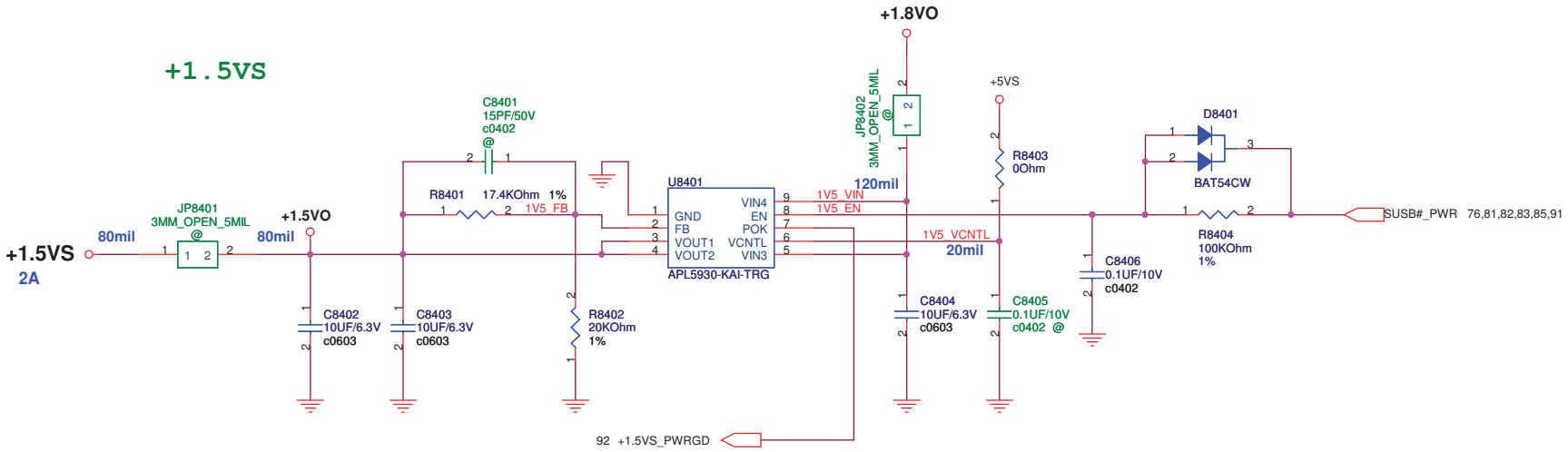
Size	Project Name	Rev
B	UX50	1.0

Date: Tuesday, March 31, 2009 Sheet 82 of 97



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_DDR & VTT	
	Engineer: Morris/Eric	
Size: Custom	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 83 of 97	

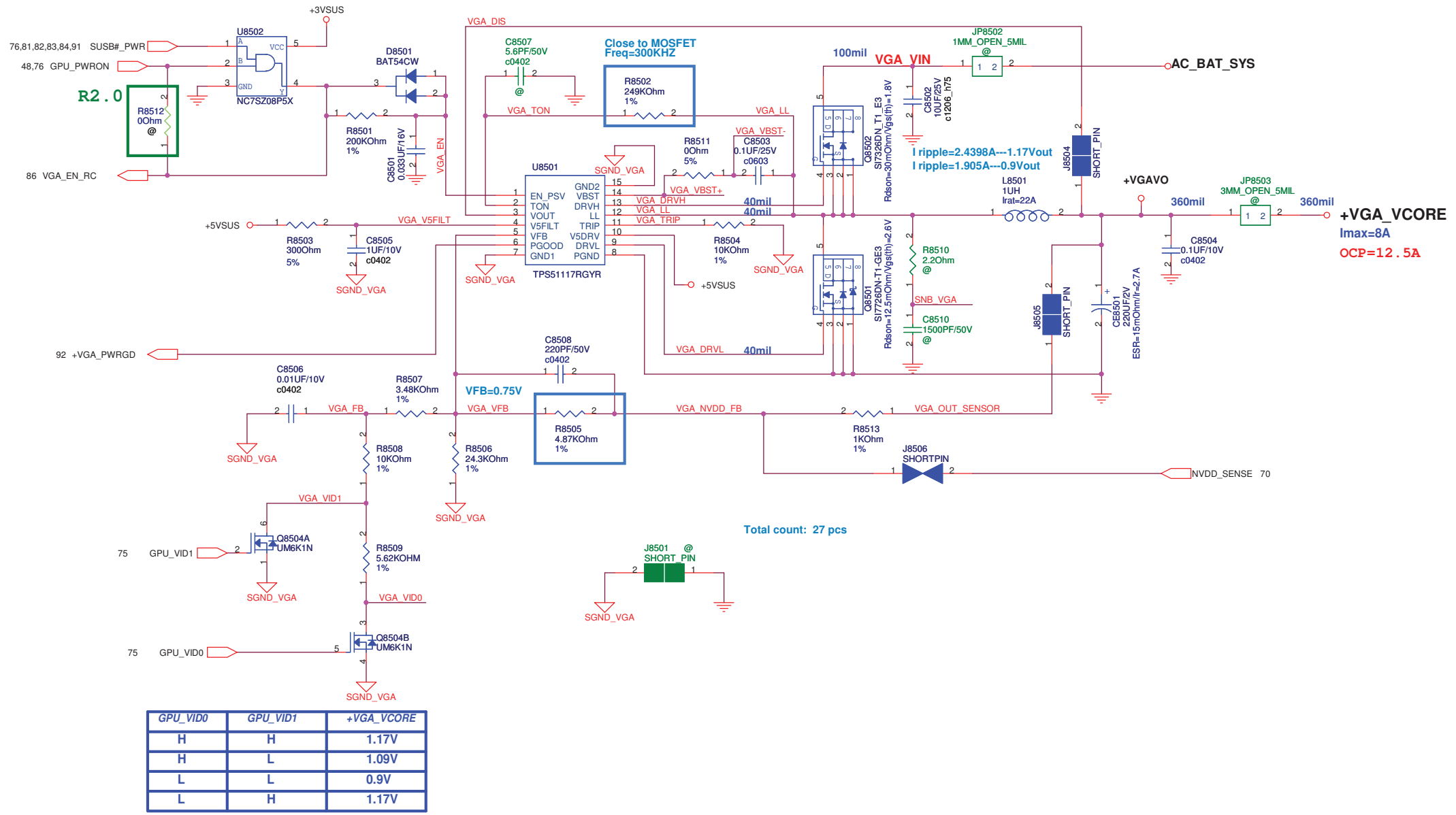


Total count: 12 pcs

LDO Second source APL5913-KAC-TRL

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+1.5VS	
	Engineer: Morris/Eric	
Size: B	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 84 of 97	



GPU_VID0	GPU_VID1	+VGA_VCORE
H	H	1.17V
H	L	1.09V
L	L	0.9V
L	H	1.17V

<Variant Name>

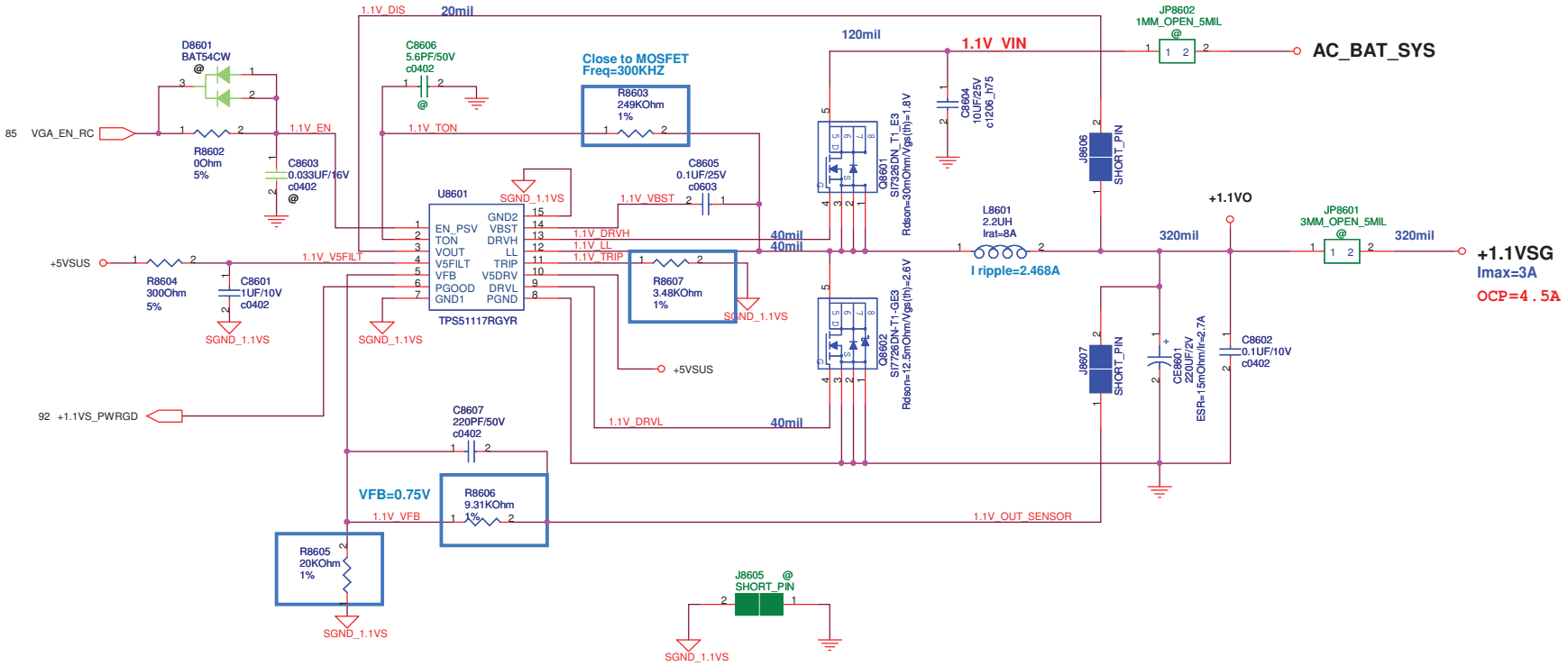
Title : POWER_I/O_VGA

ASUSTeK COMPUTER INC. NB

Engineer: Morris/Eric

Size	Project Name	Rev
B	UX50	1.0

Date: Tuesday, March 31, 2009 Sheet 85 of 97



<Variant Name>

ASUSTeK COMPUTER INC. NB

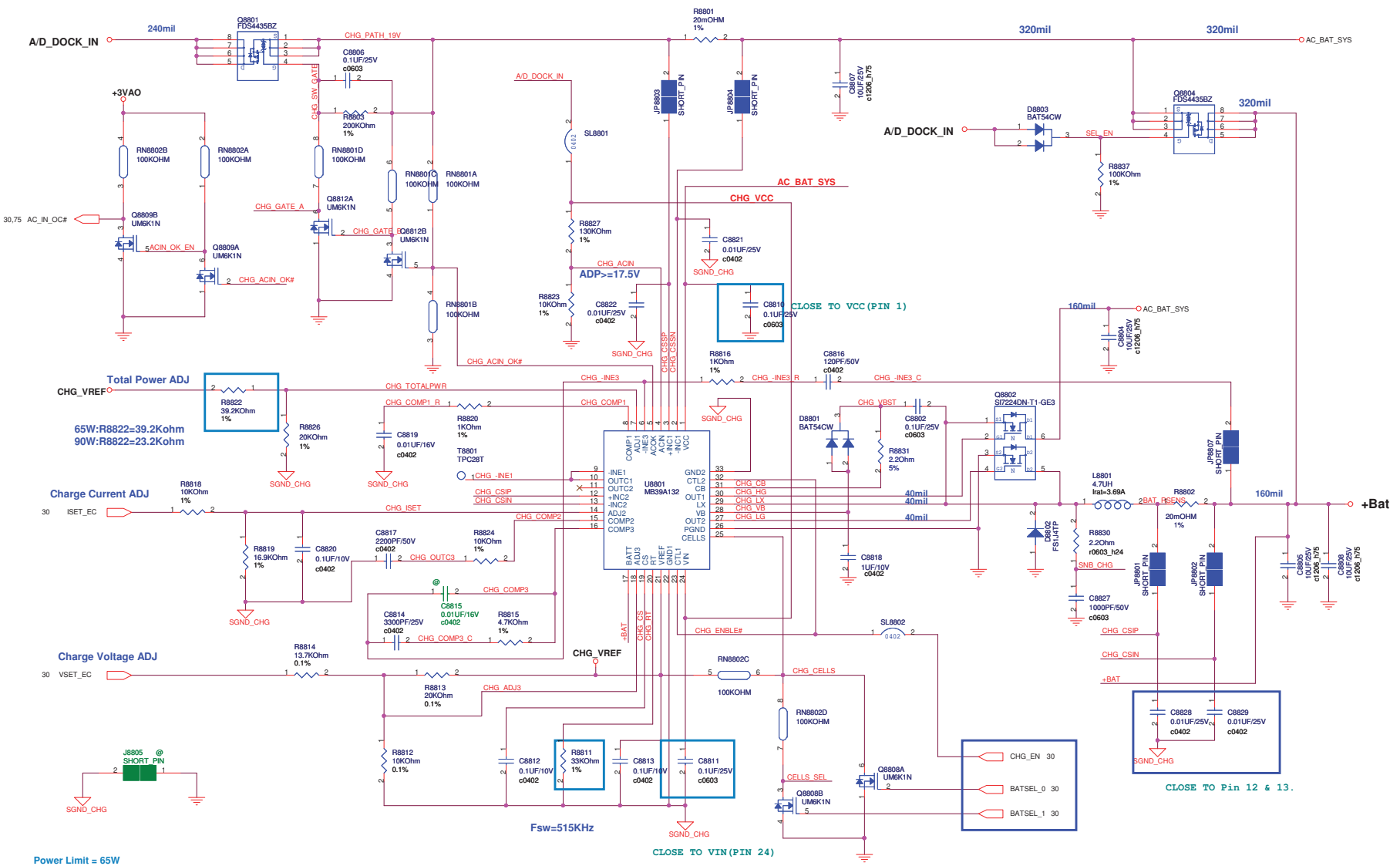
Title : POWER_I/O_1.1VS

Engineer: Morris/Eric

Size	Project Name	Rev
Custom	UX50	1.0

Date: Tuesday, March 31, 2009 Sheet 86 of 97

Title	<Title>
Size: A	Document Number: <Doc>
Rev	<RevCode>
Date:	Tuesday, March 31, 2009
Sheet	87 of 97



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Size: A	Document Number: <Doc>
Rev	<RevCode>
Date:	Tuesday, March 31, 2009
Sheet	89 of 97

BATTERY IN DETECT

<Variant Name>

ASUSTeK COMPUTER INC. NB

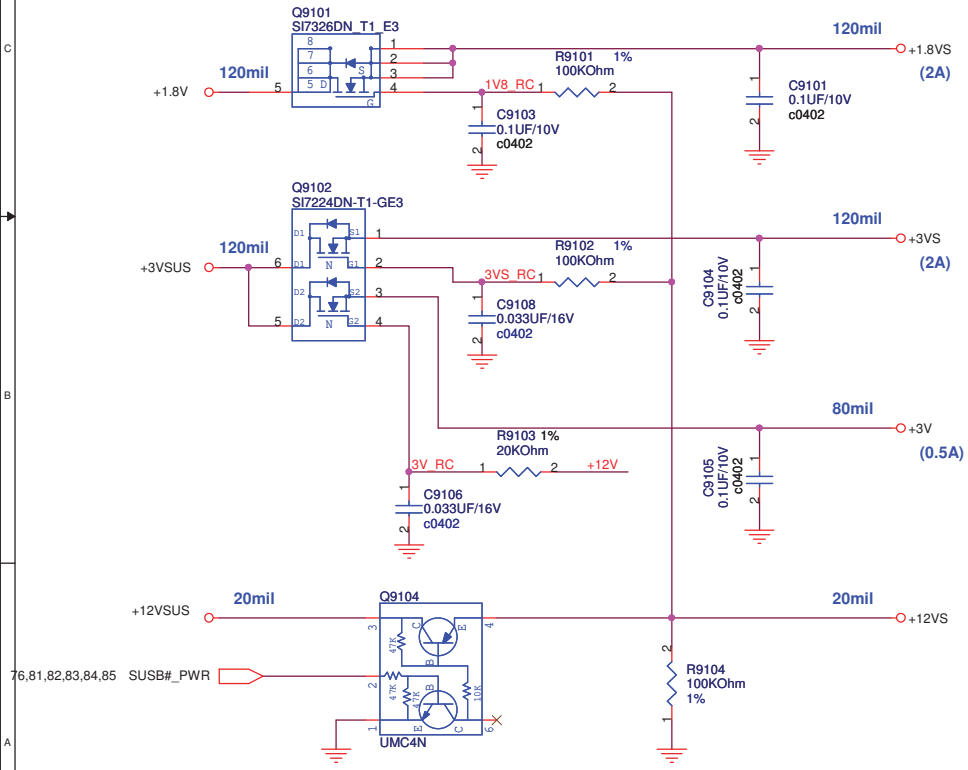
Title : POWER_DETECT

Engineer: Morris/Eric

Size	Project Name	Rev
Custom	UX50	1.0

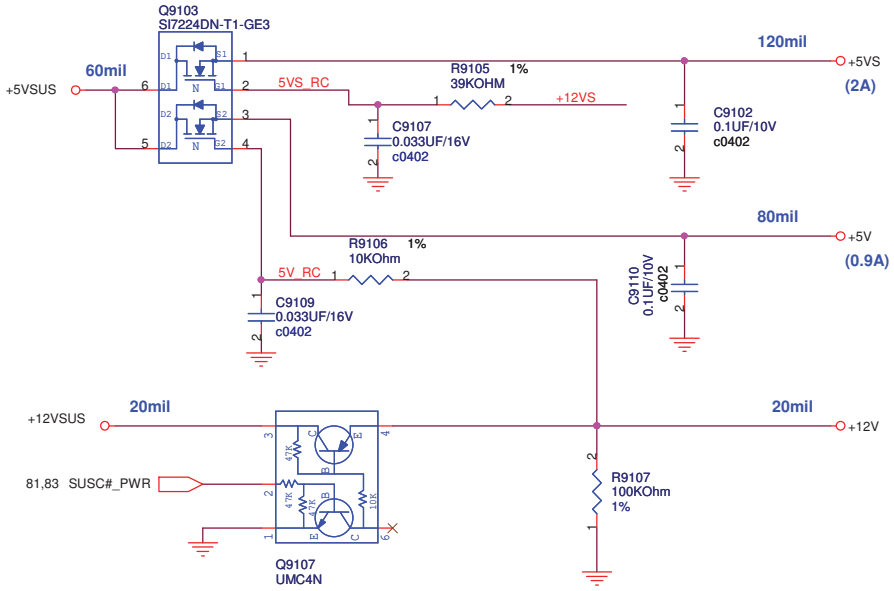
Date: Tuesday, March 31, 2009 Sheet 90 of 97

SUSB#_PWR POWER



Total count: 20 pcs

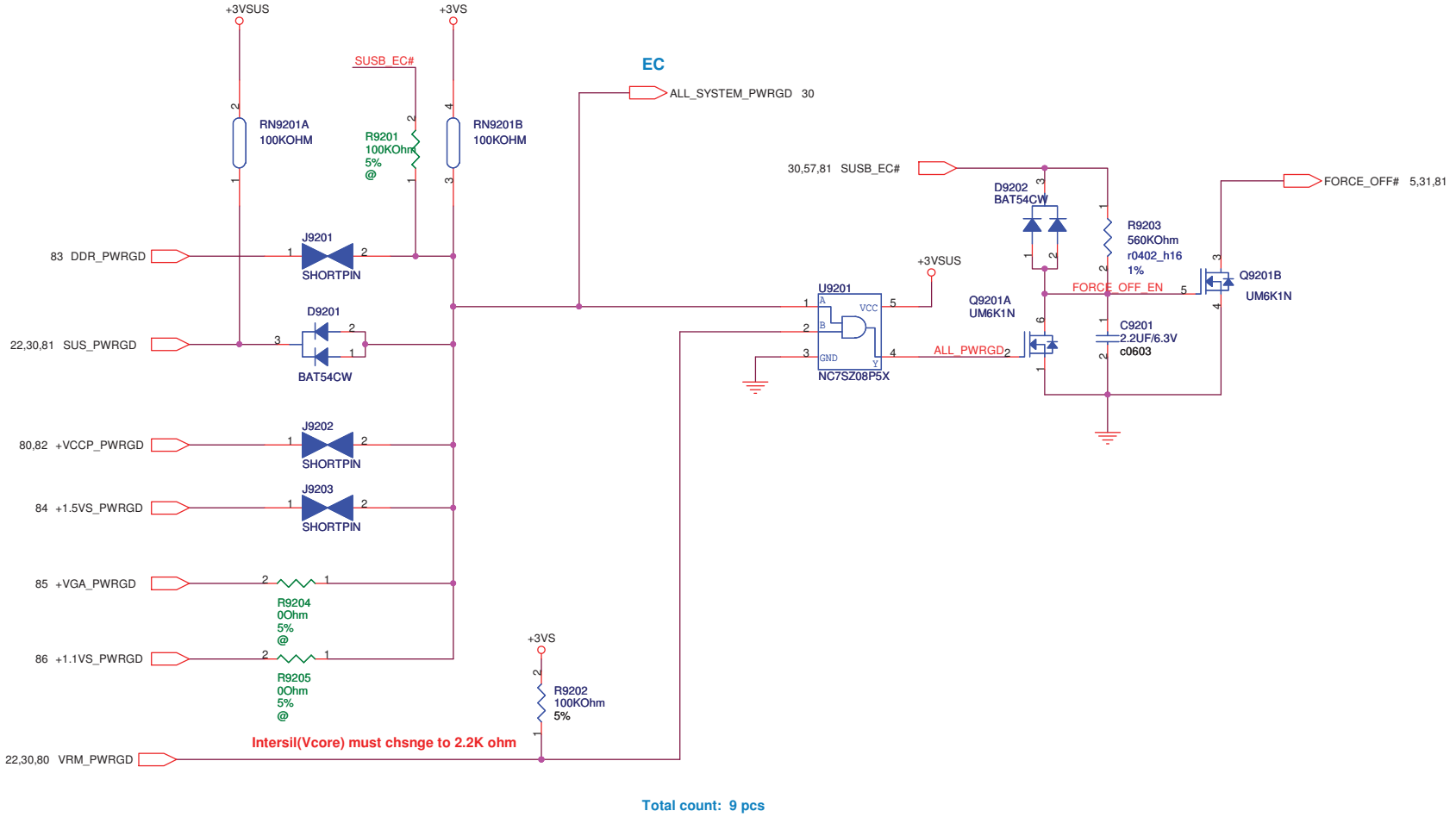
SUSC#_PWR POWER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Morris/Eric	
Size: B	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 91 of 97	

POWER GOOD DETECTER



Total count: 9 pcs

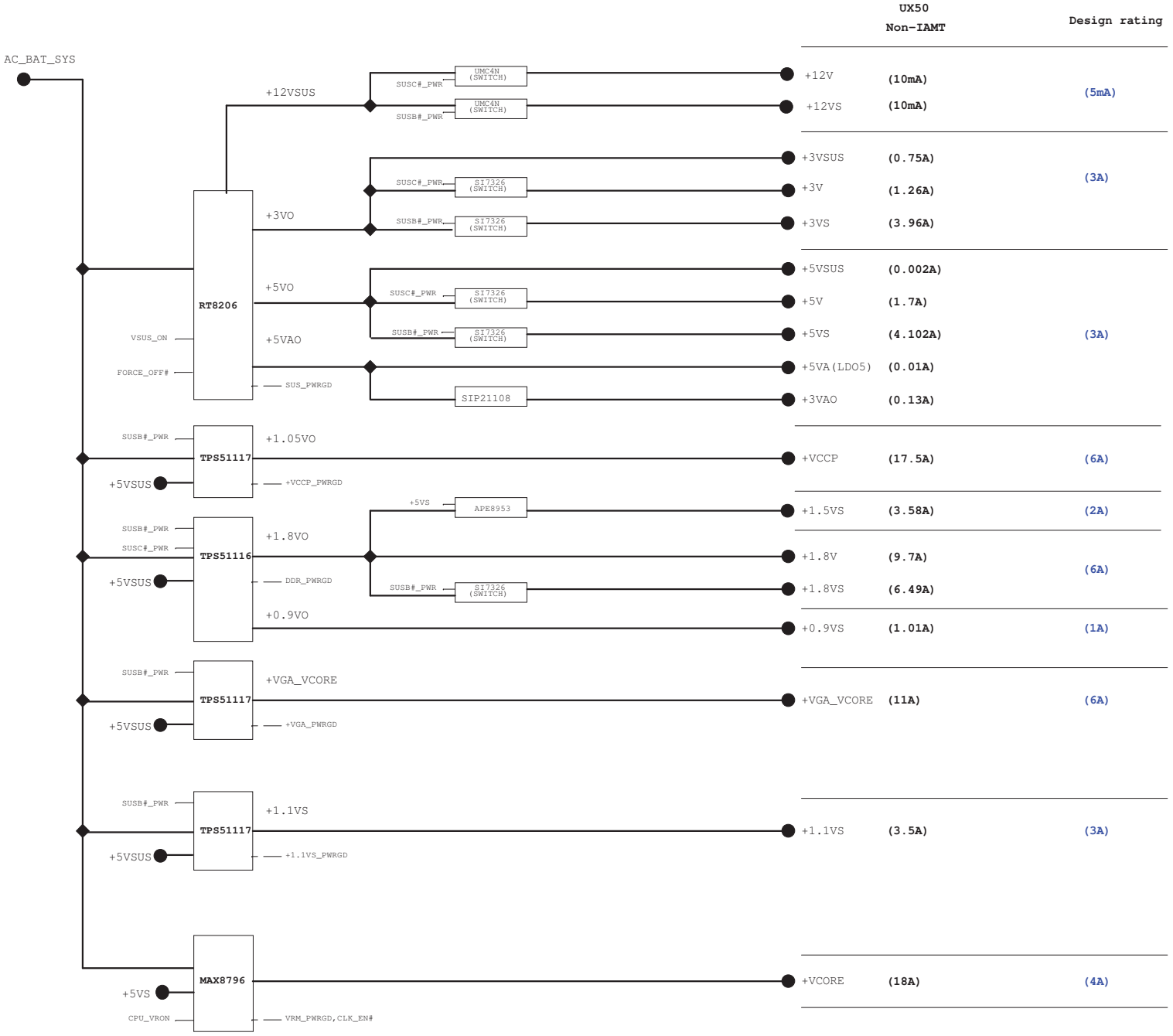
<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Morris/Eric	
Size: B	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 92 of 97	

Total sum count: 236 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_SIGNAL	
	Engineer: Morris/Eric	
Size: Custom	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 93 of 97	



UX50
Non-IAMT

Design rating

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Morris/Eric

Size: Custom | Project Name: UX50 | Rev: 1.0

Date: Tuesday, March 31, 2009 | Sheet 94 of 97

ASUSTeK COMPUTER INC. NB3	Title : POWER_CHARGER			
	Engineer: Eric_Ho			
Size: A	Project Name: UX50			Rev: 1.0
Date: Tuesday, March 31, 2009		Sheet 95 of 97		

Rev	Date	Description
1.00		First Release!
1.10	02/08/2009	1. Change net ALS_AD to J6801. (Page 68)
		2. Change RTC circuit from small board to M/B. (Page 20)
		3. Add net CLK_PCIE_VGA and CLK_PCIE_VGA#.(Page 29)
		4. Add pull-up for SMBus.(Page 22)
		5. Add ITP connector. (Page 03,29)
		6. Add MOS for dGPU power. (Page 76)
	02/10/2009	7. Change LAN PCIE to port 6. (Page 21)
		8. Add AL_LED# to control ambient light LED. (Page 30,68)
		9. Change C7036 to 4.7UF. (Page 70)
		10. Swapping DDR2 nets (Page 09,29,74)
	02/11/2009	11. Add USB port for WiMax (Page 68,21)
		12. Remove test point for layout. (Page 30)
	02/16/2009	13. Change 8pF cap for 32.768KHz crystal. (Page 20,30)
	02/17/2009	14. Swap J6801 BAT pins (Page 68)
2.00	03/04/2009	1. Remove D4503 for HDA issue. (Page 45)
	03/09/2009	2. Add HDMI hot plug detect in iGPU mode. (Page 48)
	03/09/2009	3. Add C6805 for EMI. (Page 68)
	03/12/2009	4. Change HDMI hot plug detect pin to EC GPI6. (Page 30,48)
	03/12/2009	5. Add CE0502 for CPU SU9600 hang issue. (Page 5)
	03/12/2009	6. Pull up backligh enable pin tto +3VS_LCD from +3VS. (Page 46)
	03/16/2009	7. Swap RN2917. (Page 29)
	03/18/2009	8. Change R7301 to 120ohm. (Page 73)

Title : HISTORY

<OrgName>

Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0

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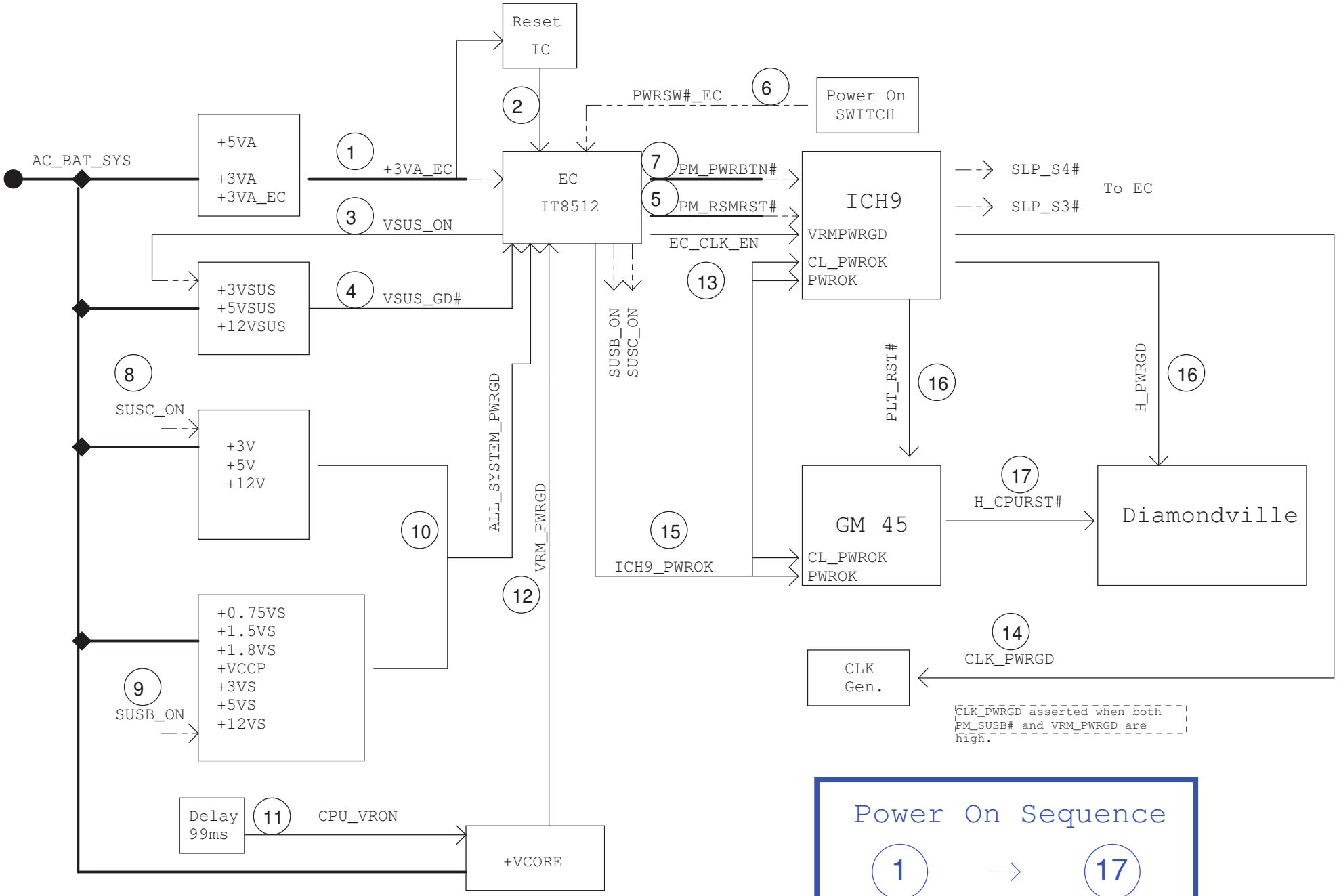

<OrgName>	Title : POWER SEQUENCE	
	Engineer: Tony Su	
Size: Custom	Project Name: UX50	Rev: 1.0
Date: Tuesday, March 31, 2009	Sheet 97 of 97	