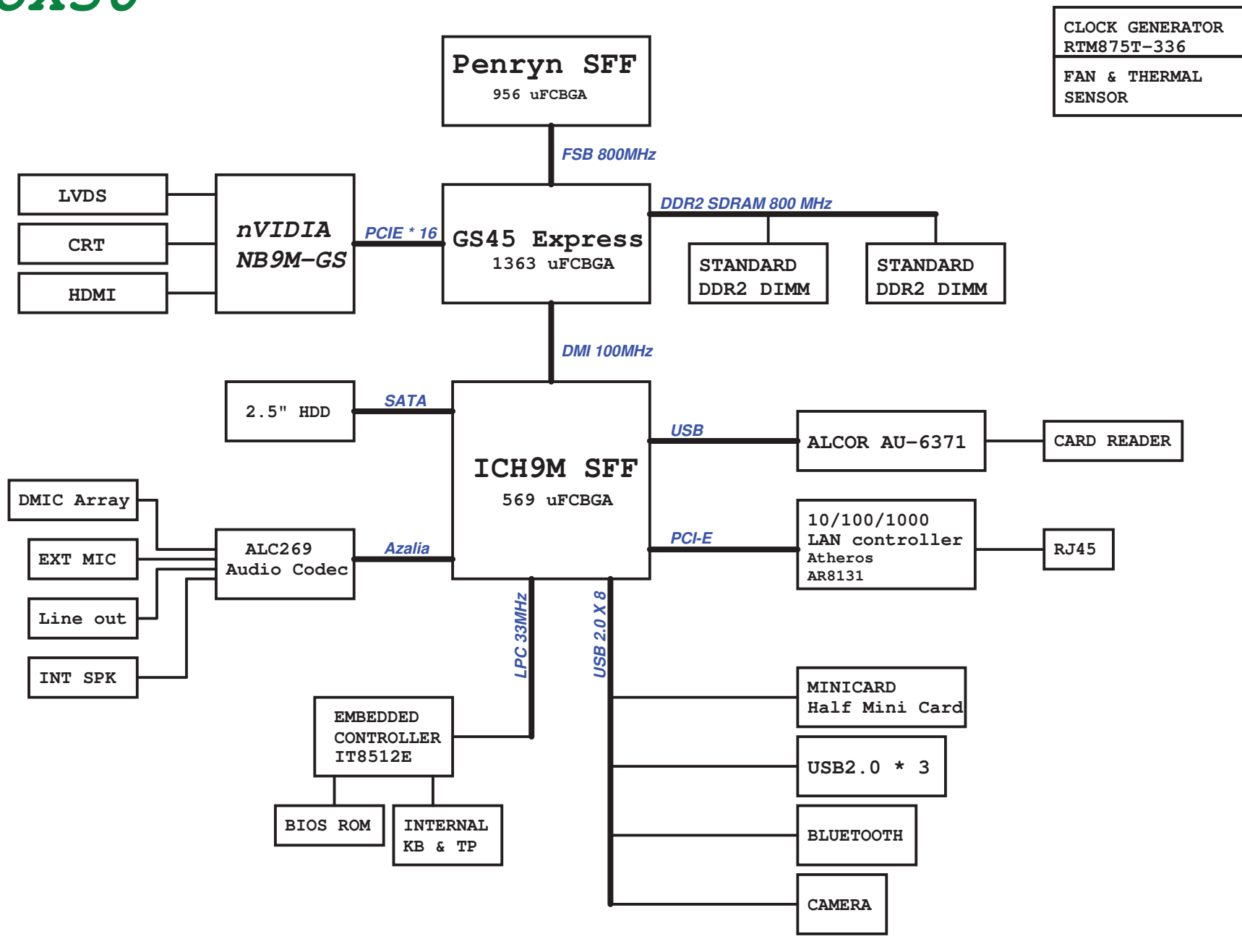




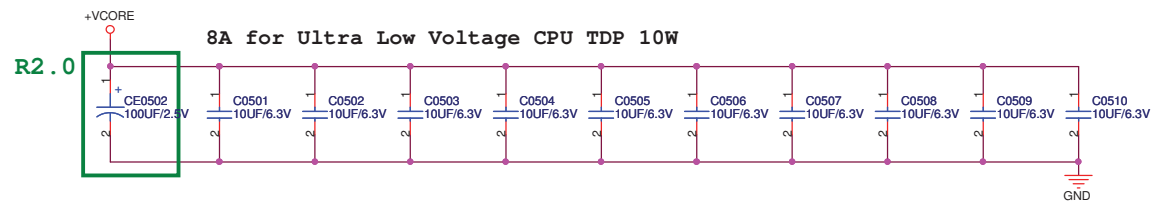
CLOCK GENERATOR
RTM875T-336

FAN & THERMAL
SENSOR

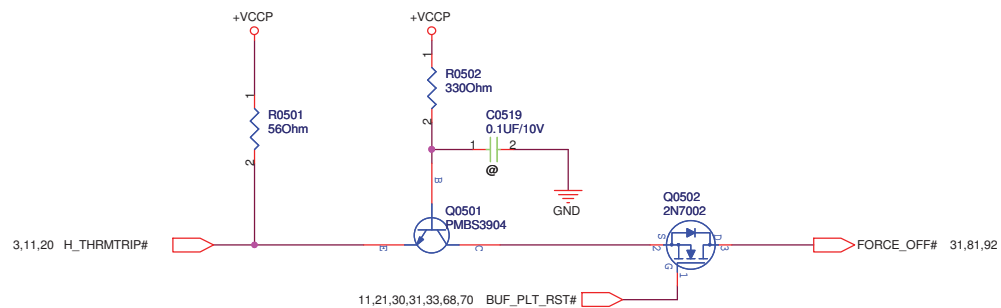
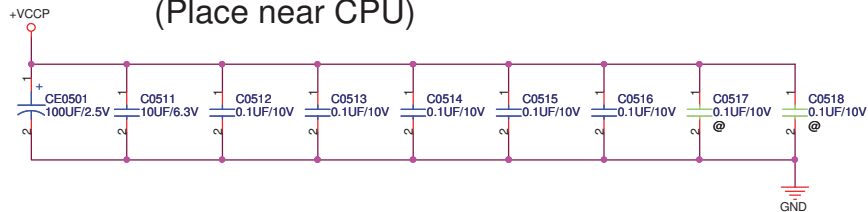
POWER

VCORE
SYSTEM
I/O_1.5VS & 1.05VS
I/O_DDR & VTT
I/O_ +1.8VS
CHARGER
LCD DRIVER

[illegible][illegible]



+VCCP Decoupling Capacitor (Place near CPU)

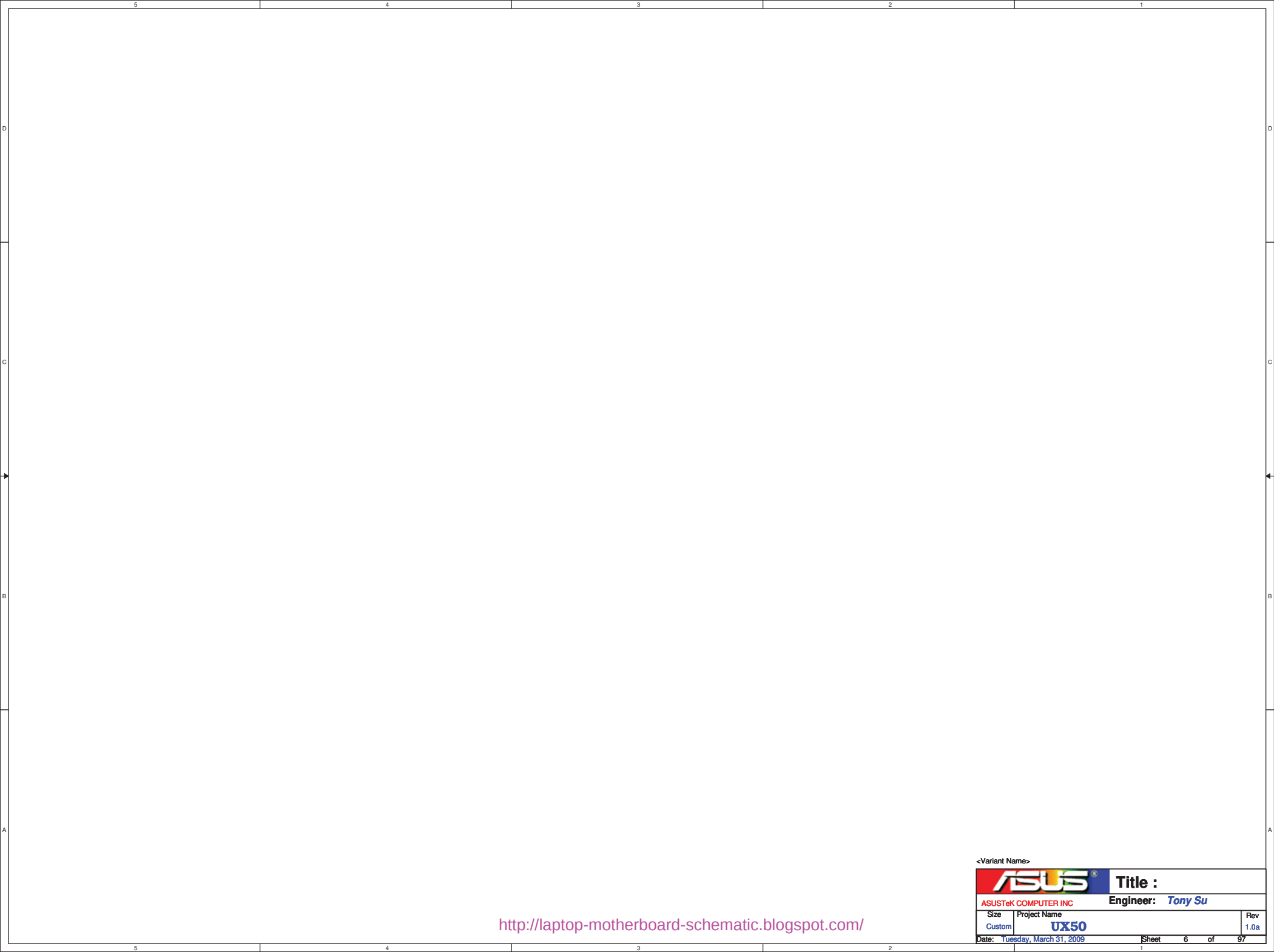


Decoupling guide from Intel

VCCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	*12pcs
	270uF	*1 pcs
VCCA	0.01uF	*1 pcs
	10uF	*1 pcs

<Variant Name>

ASUS		Title :CPU CAPACITORS	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name		
Custom	UX50	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet	5	of 97



<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

**ASUS**[®]

Title :

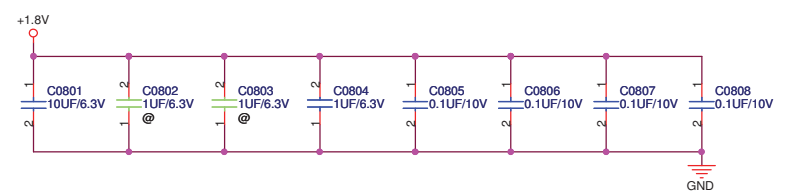
ASUSTeK COMPUTER INC

Engineer: *Tony Su*

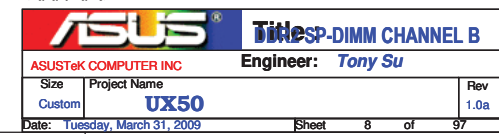
Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009

Sheet 6 of 97

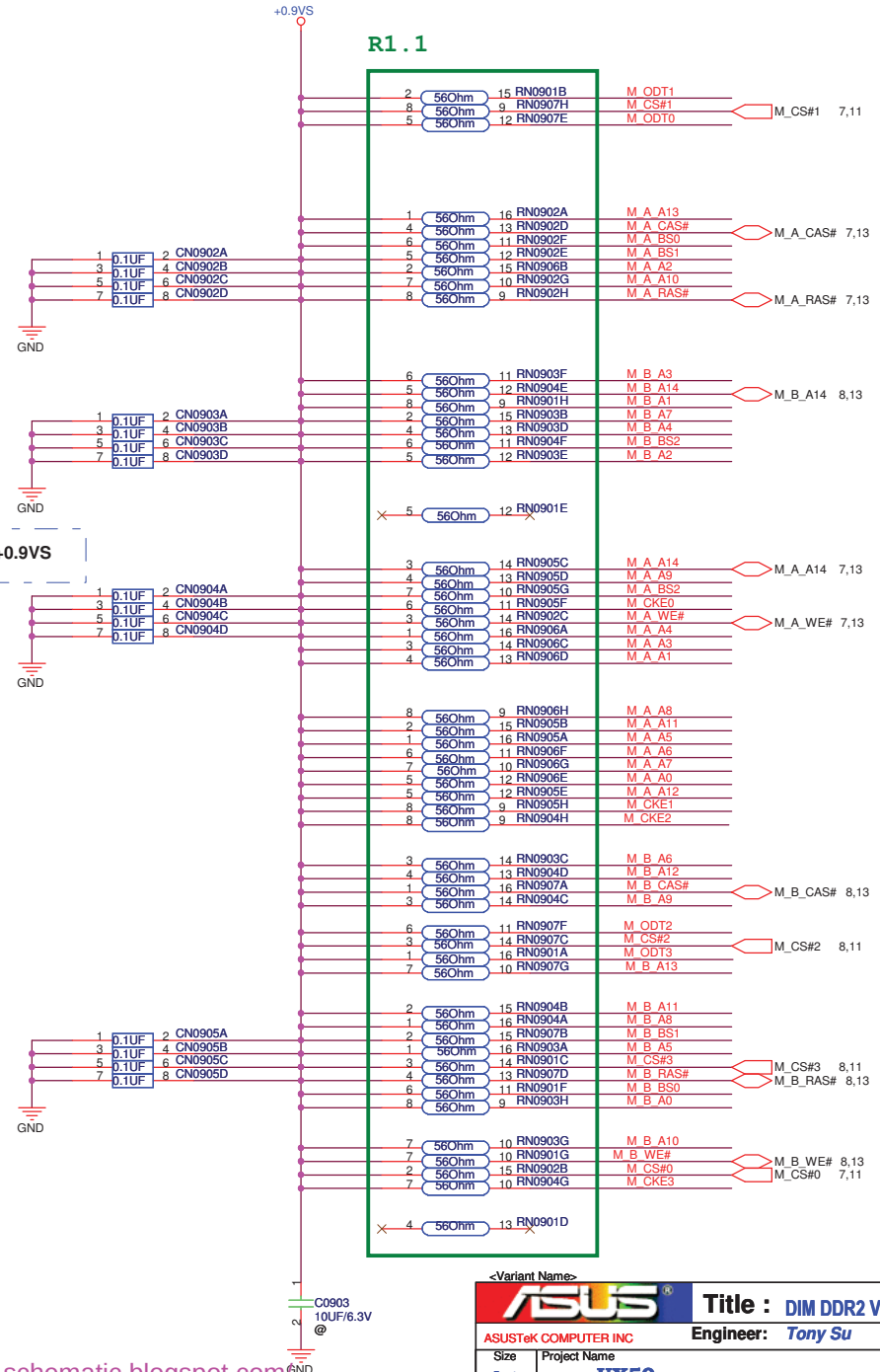


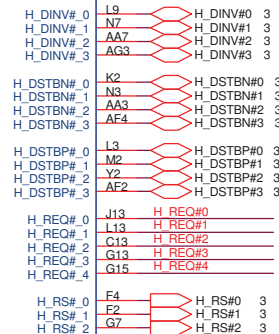
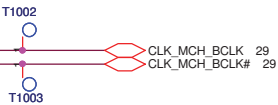
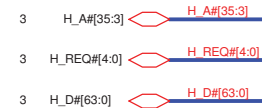
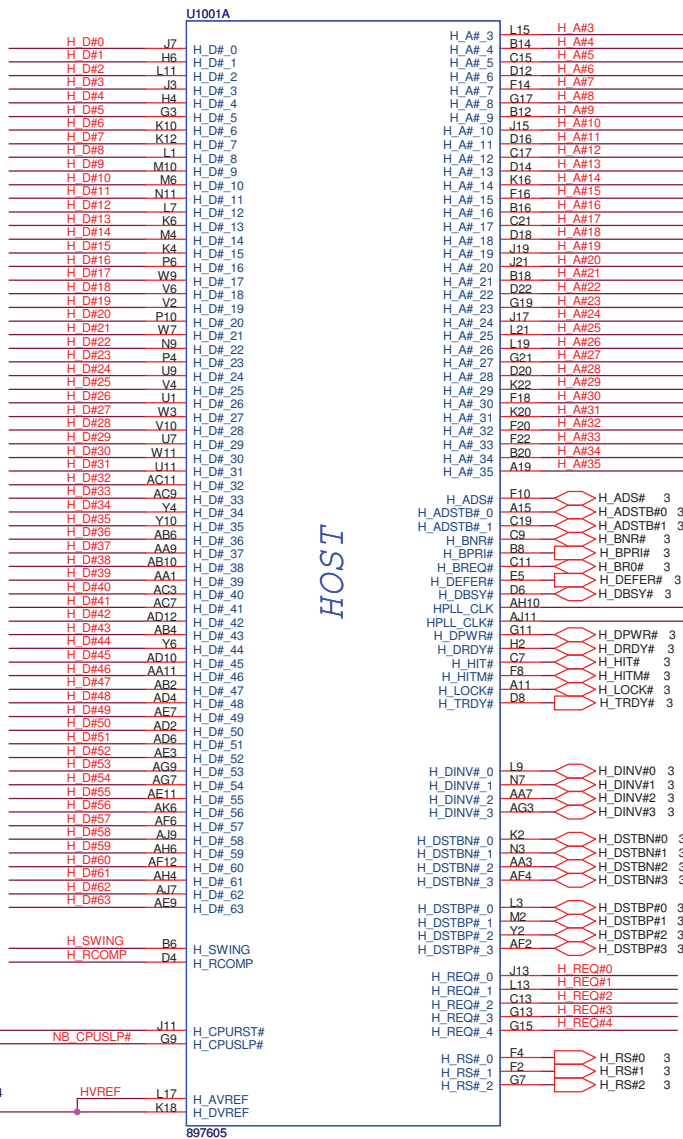
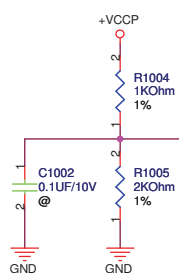
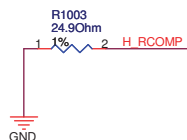
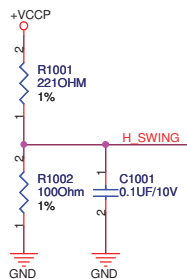
<Variant Name>



M_A_A[0..13] 7,13
M_A_BS[0..2] 7,13
M_B_A[0..13] 8,13
M_B_BS[0..2] 8,13
M_CKE[0..3] 7,8,11
M_ODT[0..3] 7,8,11

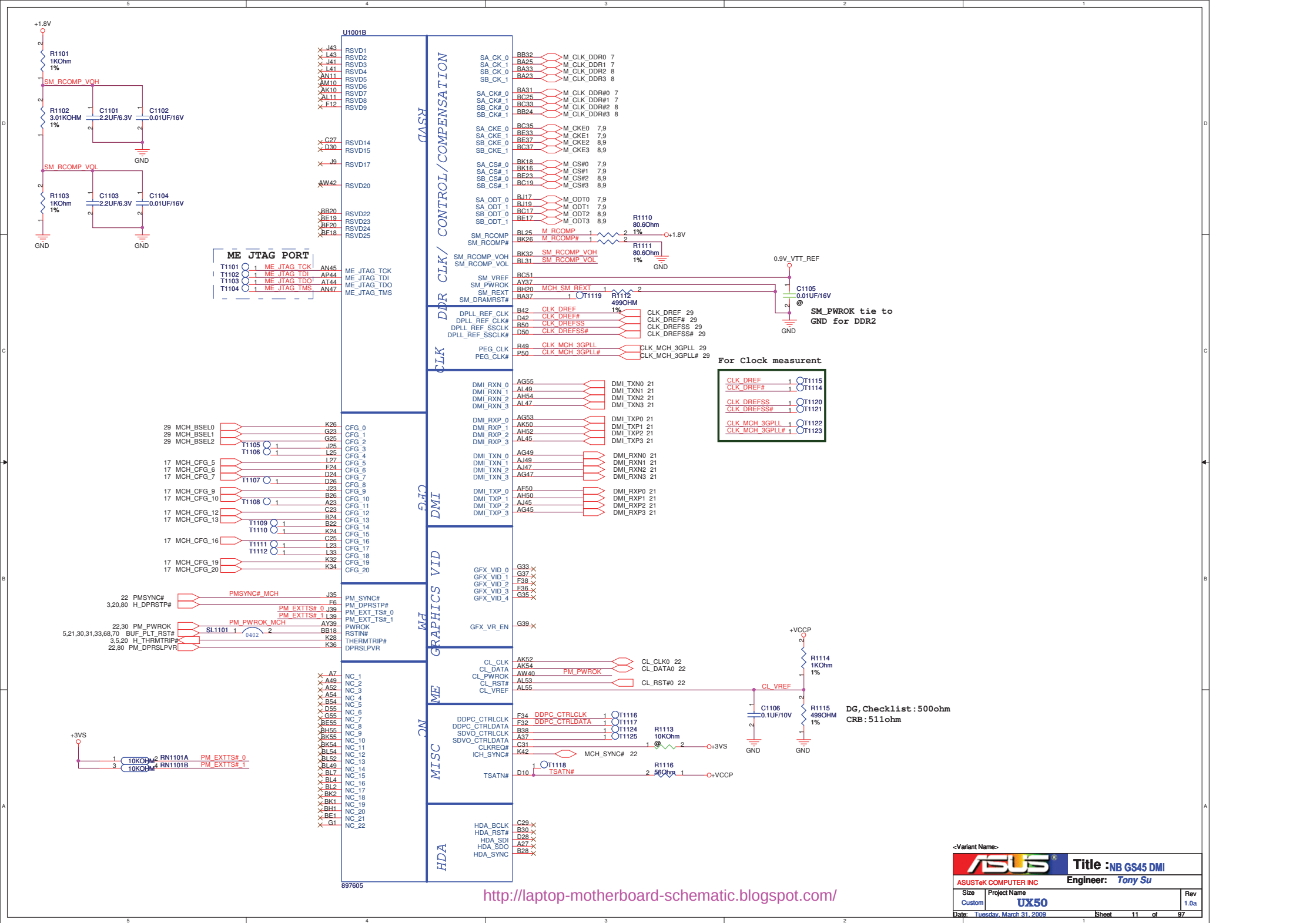
Layout note: Place array cap close to each pullup resistors terminated to +0.9VS





<Variant Name>

ASUS		Title :NB GS45 HOST	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009	Sheet	10	of 97



7 M_A_DQ[0:63]

U1001D

M A DQ0 AP46 SA DO_0
 M A DQ1 AU47 SA DO_1
 M A DQ2 AT46 SA DO_2
 M A DQ3 AU49 SA DO_3
 M A DQ4 AR45 SA DO_4
 M A DQ5 AV49 SA DO_5
 M A DQ6 AV50 SA DO_6
 M A DQ7 AP50 SA DO_7
 M A DQ8 AW47 SA DO_8
 M A DQ9 BD50 SA DO_9
 M A DQ10 AW49 SA DO_10
 M A DQ11 BA49 SA DO_11
 M A DQ12 BC49 SA DO_12
 M A DQ13 AV46 SA DO_13
 M A DQ14 BA47 SA DO_14
 M A DQ15 AY50 SA DO_15
 M A DQ16 BF46 SA DO_16
 M A DQ17 BC47 SA DO_17
 M A DQ18 BF50 SA DO_18
 M A DQ19 BF48 SA DO_19
 M A DQ20 BC43 SA DO_20
 M A DQ21 BE49 SA DO_21
 M A DQ22 BA43 SA DO_22
 M A DQ23 BE47 SA DO_23
 M A DQ24 BF42 SA DO_24
 M A DQ25 BC39 SA DO_25
 M A DQ26 BF44 SA DO_26
 M A DQ27 BF40 SA DO_27
 M A DQ28 BB40 SA DO_28
 M A DQ29 BE43 SA DO_29
 M A DQ30 BF38 SA DO_30
 M A DQ31 BE41 SA DO_31
 M A DQ32 BA15 SA DO_32
 M A DQ33 BE11 SA DO_33
 M A DQ34 BE15 SA DO_34
 M A DQ35 BE14 SA DO_35
 M A DQ36 BE14 SA DO_36
 M A DQ37 BC15 SA DO_37
 M A DQ38 BE13 SA DO_38
 M A DQ39 BE16 SA DO_39
 M A DQ40 BE10 SA DO_40
 M A DQ41 BC11 SA DO_41
 M A DQ42 BF8 SA DO_42
 M A DQ43 BG7 SA DO_43
 M A DQ44 BC7 SA DO_44
 M A DQ45 BC9 SA DO_45
 M A DQ46 BD6 SA DO_46
 M A DQ47 BF12 SA DO_47
 M A DQ48 AV6 SA DO_48
 M A DQ49 BB6 SA DO_49
 M A DQ50 AW7 SA DO_50
 M A DQ51 AY6 SA DO_51
 M A DQ52 AT10 SA DO_52
 M A DQ53 AW11 SA DO_53
 M A DQ54 AU11 SA DO_54
 M A DQ55 AW9 SA DO_55
 M A DQ56 AR11 SA DO_56
 M A DQ57 AT6 SA DO_57
 M A DQ58 AP6 SA DO_58
 M A DQ59 AL7 SA DO_59
 M A DQ60 AR7 SA DO_60
 M A DQ61 AT12 SA DO_61
 M A DQ62 AM6 SA DO_62
 M A DQ63 AU7 SA DO_63

DDR SYSTEM MEMORY A

SA_BS_0
 SA_BS_1
 SA_BS_2
 SA_RAS#
 SA_CAS#
 SA_WE#

BC21 M A BS0 7,9
 BJ21 M A BS1 7,9
 BJ41 M A BS2 7,9
 BH22 M A RAS# 7,9
 BK20 M A CAS# 7,9
 BL15 M A WE# 7,9

SA_DM_0
 SA_DM_1
 SA_DM_2
 SA_DM_3
 SA_DM_4
 SA_DM_5
 SA_DM_6
 SA_DM_7

AT50 M A DM0
 BB50 M A DM1
 BB46 M A DM2
 BE39 M A DM3
 BB12 M A DM4
 BE7 M A DM5
 AV10 M A DM6
 AR9 M A DM7

SA_DQS_0
 SA_DQS_1
 SA_DQS_2
 SA_DQS_3
 SA_DQS_4
 SA_DQS_5
 SA_DQS_6
 SA_DQS_7

AR47 M A DQS0
 BA45 M A DQS1
 BE45 M A DQS2
 BC41 M A DQS3
 BC13 M A DQS4
 BB10 M A DQS5
 BA7 M A DQS6
 AN7 M A DQS7
 AR49 M A DQS#0
 AW45 M A DQS#1
 BC45 M A DQS#2
 BA41 M A DQS#3
 BA13 M A DQS#4
 BA11 M A DQS#5
 BA9 M A DQS#6
 AN9 M A DQS#7

SA_MA_0
 SA_MA_1
 SA_MA_2
 SA_MA_3
 SA_MA_4
 SA_MA_5
 SA_MA_6
 SA_MA_7
 SA_MA_8
 SA_MA_9
 SA_MA_10
 SA_MA_11
 SA_MA_12
 SA_MA_13
 SA_MA_14

BC23 M A A0
 BF22 M A A1
 BE31 M A A2
 BC31 M A A3
 BH26 M A A4
 BJ35 M A A5
 BB34 M A A6
 BH32 M A A7
 BB26 M A A8
 BF32 M A A9
 BA21 M A A10
 BG25 M A A11
 BH34 M A A12
 BH18 M A A13
 BE25 M A A14

897605

8 M_B_DQ[0:63]

U1001E

M B DQ0 AP54 SB DO_0
 M B DQ1 AM52 SB DO_1
 M B DQ2 AR55 SB DO_2
 M B DQ3 AV54 SB DO_3
 M B DQ4 AU54 SB DO_4
 M B DQ5 AN53 SB DO_5
 M B DQ6 AT52 SB DO_6
 M B DQ7 AU53 SB DO_7
 M B DQ8 AW53 SB DO_8
 M B DQ9 AY52 SB DO_9
 M B DQ10 BB52 SB DO_10
 M B DQ11 BC53 SB DO_11
 M B DQ12 AV52 SB DO_12
 M B DQ13 AW55 SB DO_13
 M B DQ14 BD52 SB DO_14
 M B DQ15 BC55 SB DO_15
 M B DQ16 BF54 SB DO_16
 M B DQ17 BE51 SB DO_17
 M B DQ18 BH48 SB DO_18
 M B DQ19 BK48 SB DO_19
 M B DQ20 BE53 SB DO_20
 M B DQ21 BH52 SB DO_21
 M B DQ22 BK46 SB DO_22
 M B DQ23 BJ47 SB DO_23
 M B DQ24 BL45 SB DO_24
 M B DQ25 BJ45 SB DO_25
 M B DQ26 BJ45 SB DO_26
 M B DQ27 BH44 SB DO_27
 M B DQ28 BH46 SB DO_28
 M B DQ29 BK44 SB DO_29
 M B DQ30 BK40 SB DO_30
 M B DQ31 BJ39 SB DO_31
 M B DQ32 BK10 SB DO_32
 M B DQ33 BH10 SB DO_33
 M B DQ34 BK6 SB DO_34
 M B DQ35 BH6 SB DO_35
 M B DQ36 BJ9 SB DO_36
 M B DQ37 BL11 SB DO_37
 M B DQ38 BG5 SB DO_38
 M B DQ39 BJ5 SB DO_39
 M B DQ40 BF4 SB DO_40
 M B DQ41 BF4 SB DO_41
 M B DQ42 BD4 SB DO_42
 M B DQ43 BA3 SB DO_43
 M B DQ44 BE5 SB DO_44
 M B DQ45 BF2 SB DO_45
 M B DQ46 BB4 SB DO_46
 M B DQ47 AY4 SB DO_47
 M B DQ48 BA1 SB DO_48
 M B DQ49 AP2 SB DO_49
 M B DQ50 AU1 SB DO_50
 M B DQ51 AT2 SB DO_51
 M B DQ52 AT4 SB DO_52
 M B DQ53 AV4 SB DO_53
 M B DQ54 AU3 SB DO_54
 M B DQ55 AR3 SB DO_55
 M B DQ56 AN1 SB DO_56
 M B DQ57 AP4 SB DO_57
 M B DQ58 AL3 SB DO_58
 M B DQ59 AJ1 SB DO_59
 M B DQ60 AK4 SB DO_60
 M B DQ61 AM4 SB DO_61
 M B DQ62 AH2 SB DO_62
 M B DQ63 AK2 SB DO_63

DDR SYSTEM MEMORY B

SB_BS_0
 SB_BS_1
 SB_BS_2

BJ13 M B BS0 8,9
 BK12 M B BS1 8,9
 BK38 M B BS2 8,9

SB_RAS#
 SB_CAS#
 SB_WE#

BE21 M B RAS# 8,9
 BH14 M B CAS# 8,9
 BK14 M B WE# 8,9

SB_DM_0
 SB_DM_1
 SB_DM_2
 SB_DM_3
 SB_DM_4
 SB_DM_5
 SB_DM_6
 SB_DM_7

AP52 M B DM0
 AY54 M B DM1
 BJ49 M B DM2
 BJ43 M B DM3
 BH12 M B DM4
 BD2 M B DM5
 AY2 M B DM6
 AJ3 M B DM7

SB_DQS_0
 SB_DQS_1
 SB_DQS_2
 SB_DQS_3
 SB_DQS_4
 SB_DQS_5
 SB_DQS_6
 SB_DQS_7

AR53 M B DQS0
 BA53 M B DQS1
 BH50 M B DQS2
 BK42 M B DQS3
 BH8 M B DQS4
 BB2 M B DQS5
 AV2 M B DQS6
 AM2 M B DQS7
 AT54 M B DQS#0
 BB54 M B DQS#1
 BJ51 M B DQS#2
 BH42 M B DQS#3
 BK8 M B DQS#4
 BC3 M B DQS#5
 AW3 M B DQS#6
 AN3 M B DQS#7

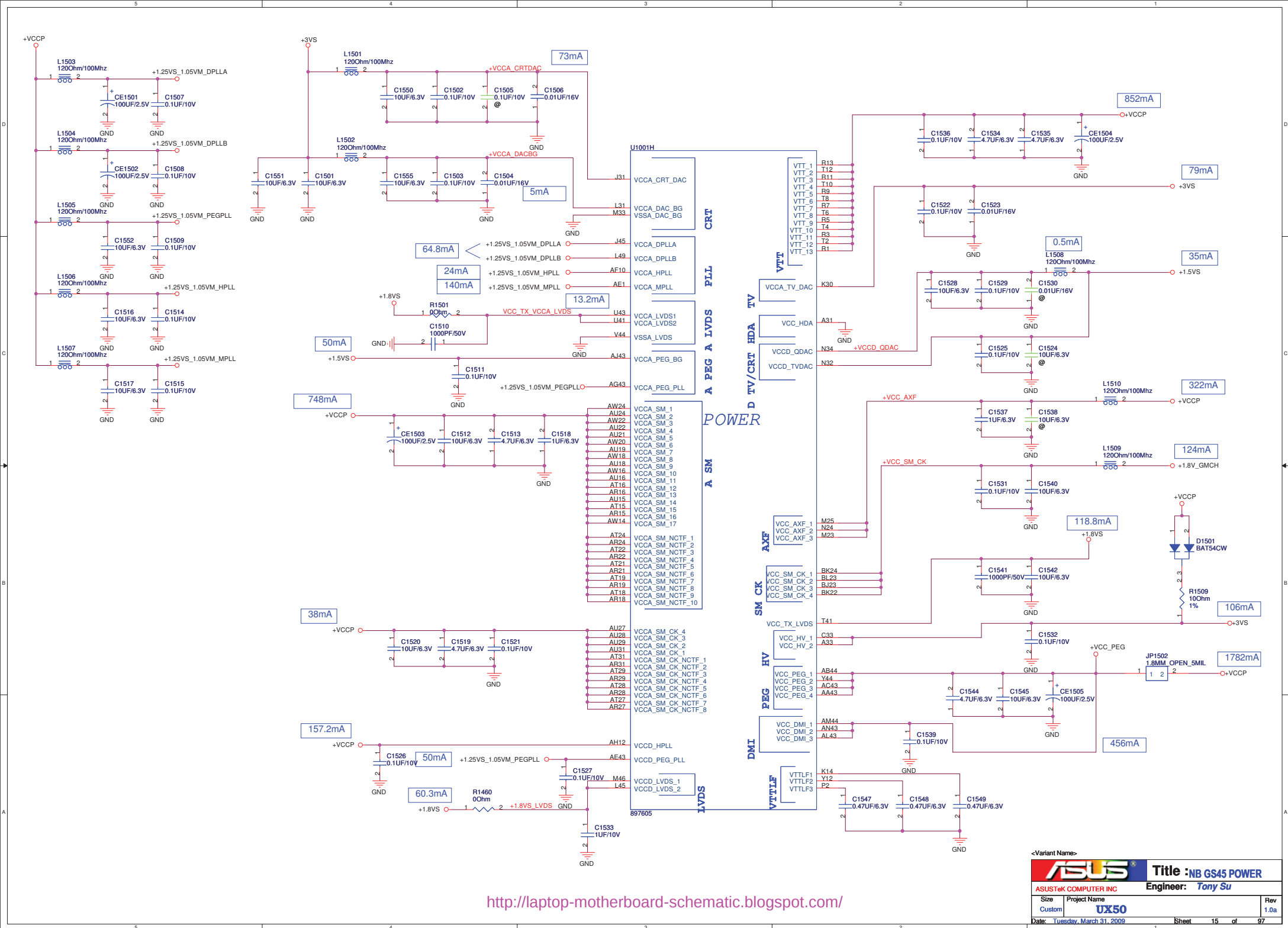
SB_MA_0
 SB_MA_1
 SB_MA_2
 SB_MA_3
 SB_MA_4
 SB_MA_5
 SB_MA_6
 SB_MA_7
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 SB_MA_9
 SB_MA_10
 SB_MA_11
 SB_MA_12
 SB_MA_13
 SB_MA_14

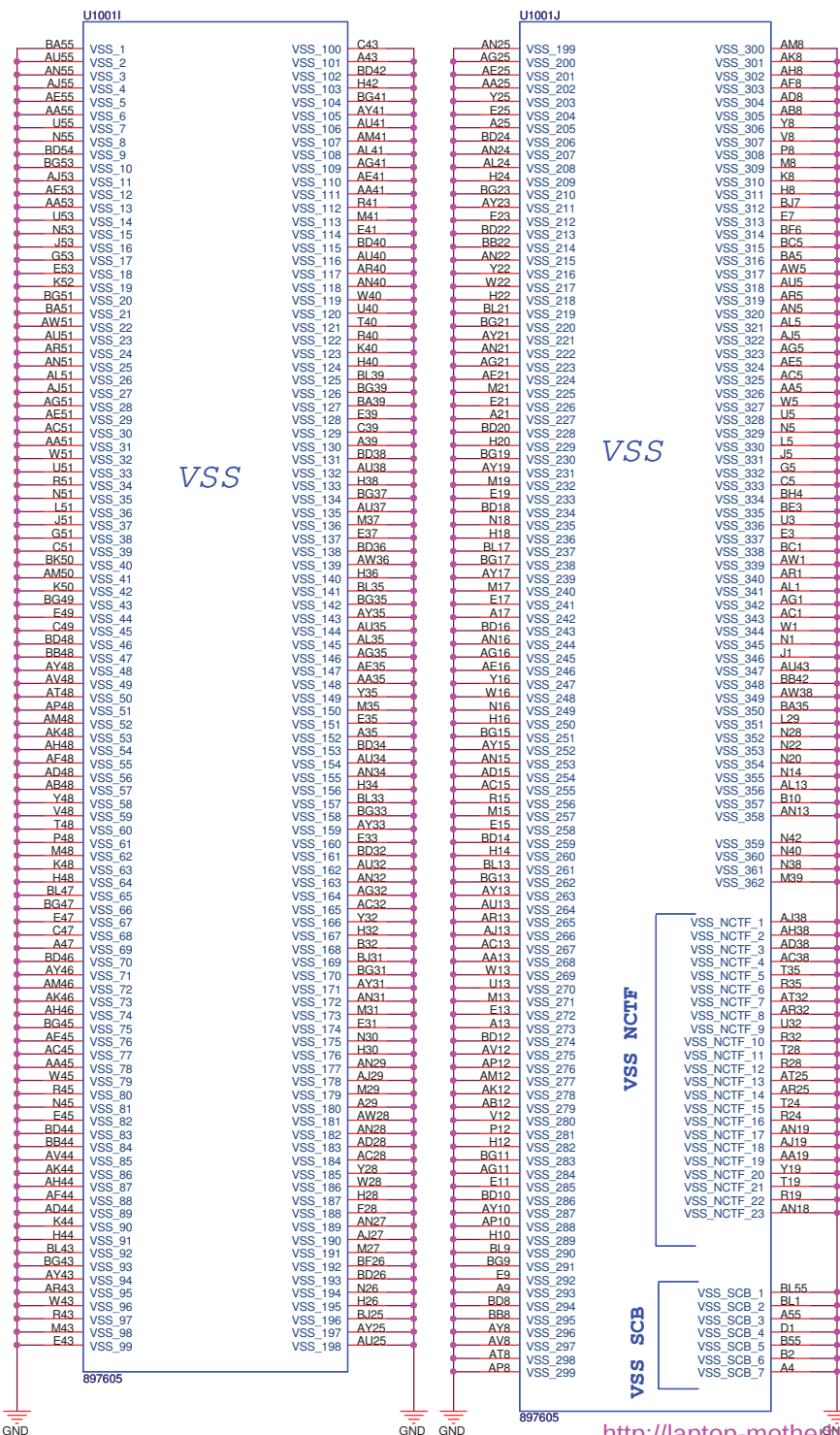
BJ15 M B A0
 BJ33 M B A1
 BH24 M B A2
 BA17 M B A3
 BF36 M B A4
 BH36 M B A5
 BF34 M B A6
 BK34 M B A7
 BJ37 M B A8
 BH40 M B A9
 BH16 M B A10
 BK36 M B A11
 BH38 M B A12
 BJ11 M B A13
 BL37 M B A14

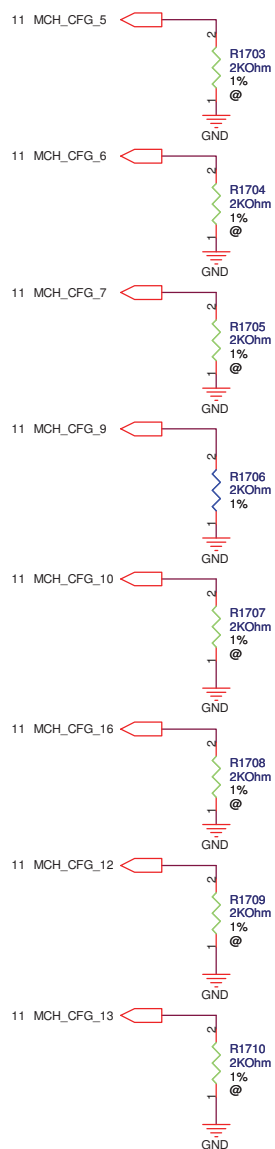
897605

<Variant Name>

ASUS		Title :NB GS45 DDR3 BUS	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size Custom	Project Name UX50		Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet	13 of	97







CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface
(Relate to SPL_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

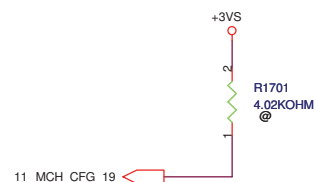
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

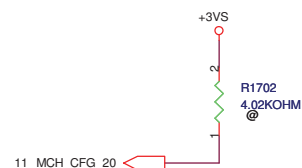
CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
 00 = Reserved
 01= XOR Mode Enabled
 10= All-Z Mode Enabled
11= Normal Operation (Default)



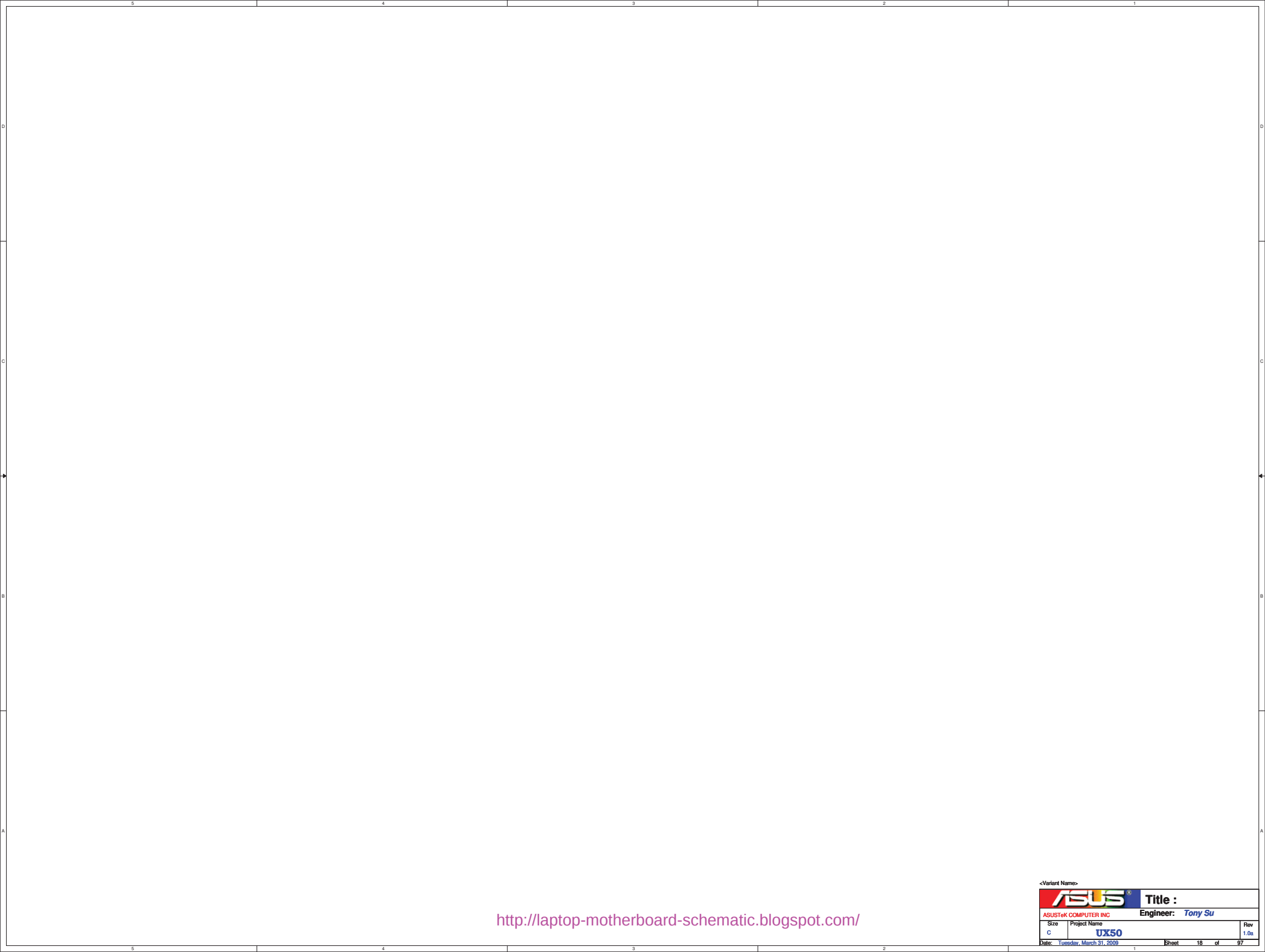
CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUS		Title :NB GS45 STRAPPING	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size Custom	Project Name UX50		Rev 1.0a
Date: Monday, April 06, 2009	Sheet	17	of 97



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-Variant Name>

**ASUS**[®]

ASUSTeK COMPUTER INC

Size
C

Project Name
UX50

Date: **Tuesday, March 31, 2009**

Title :
Engineer: **Tony Su**

Rev
1.0a

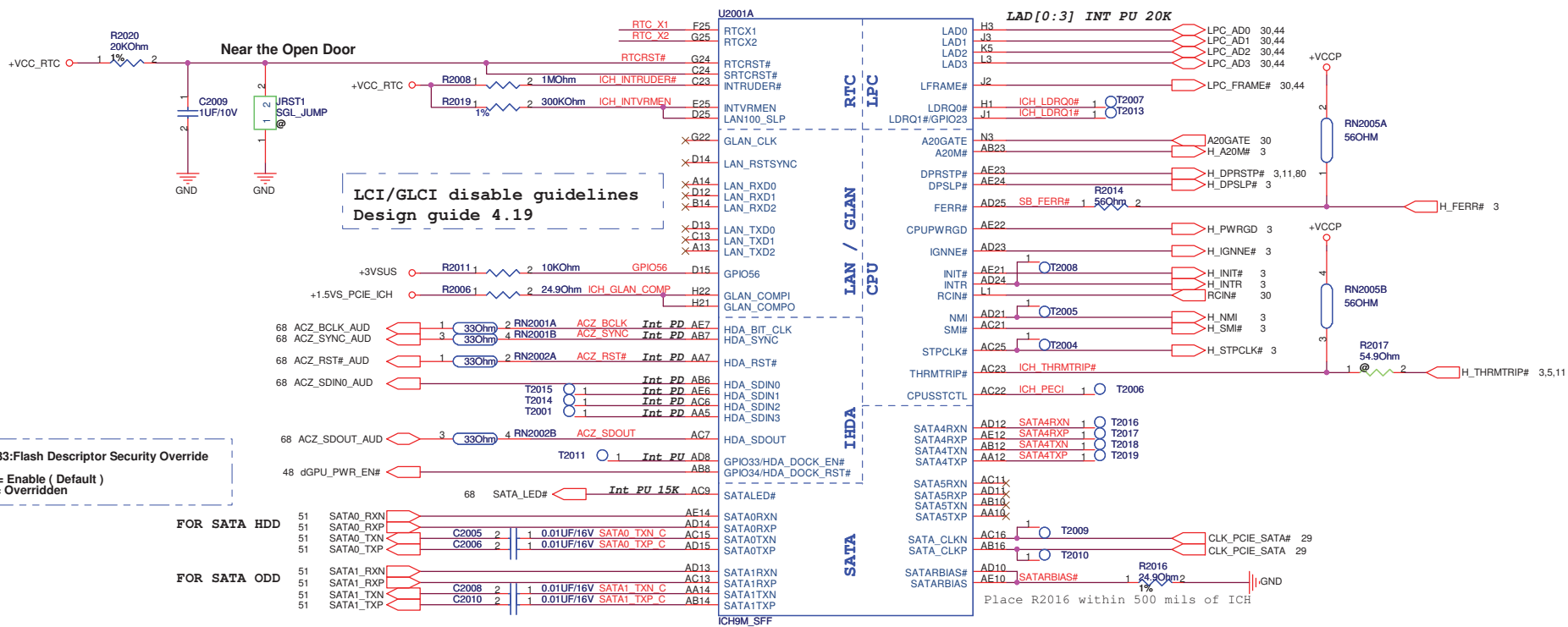
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<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet	19 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

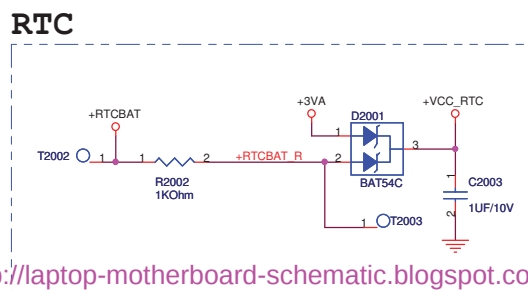
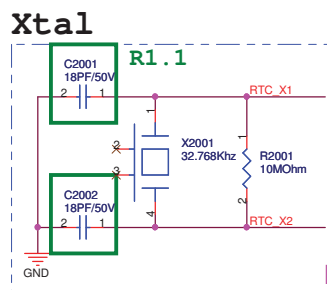


Xtal

RTC

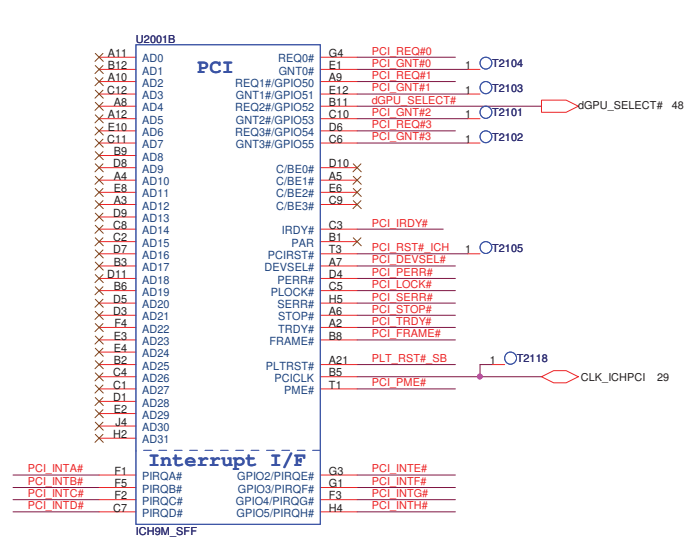
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (Default)
11 = Set PCIe Port Config Bit 1

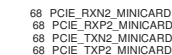


<http://laptop-motherboard-schematic.blogspot.com/>

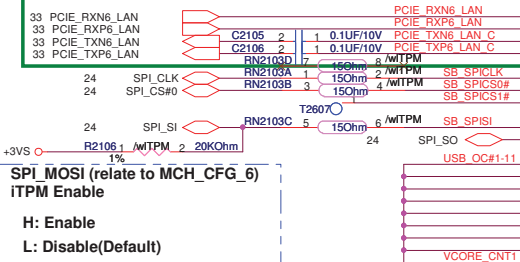
<Variant Name>



PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	GLAN



R1.1



PCI-Express

USB

USB INT PD 15K

ICH9M_SFF

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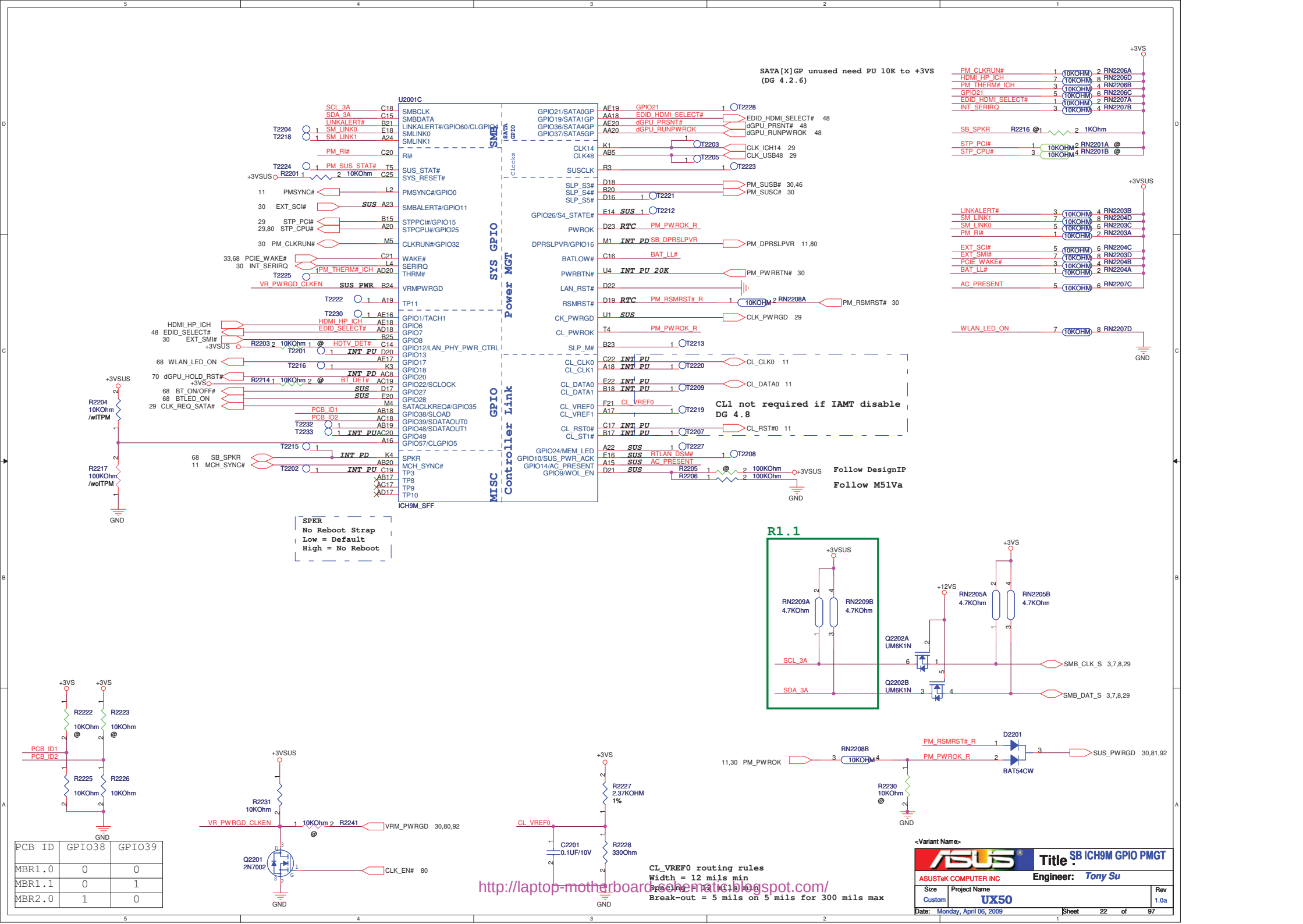
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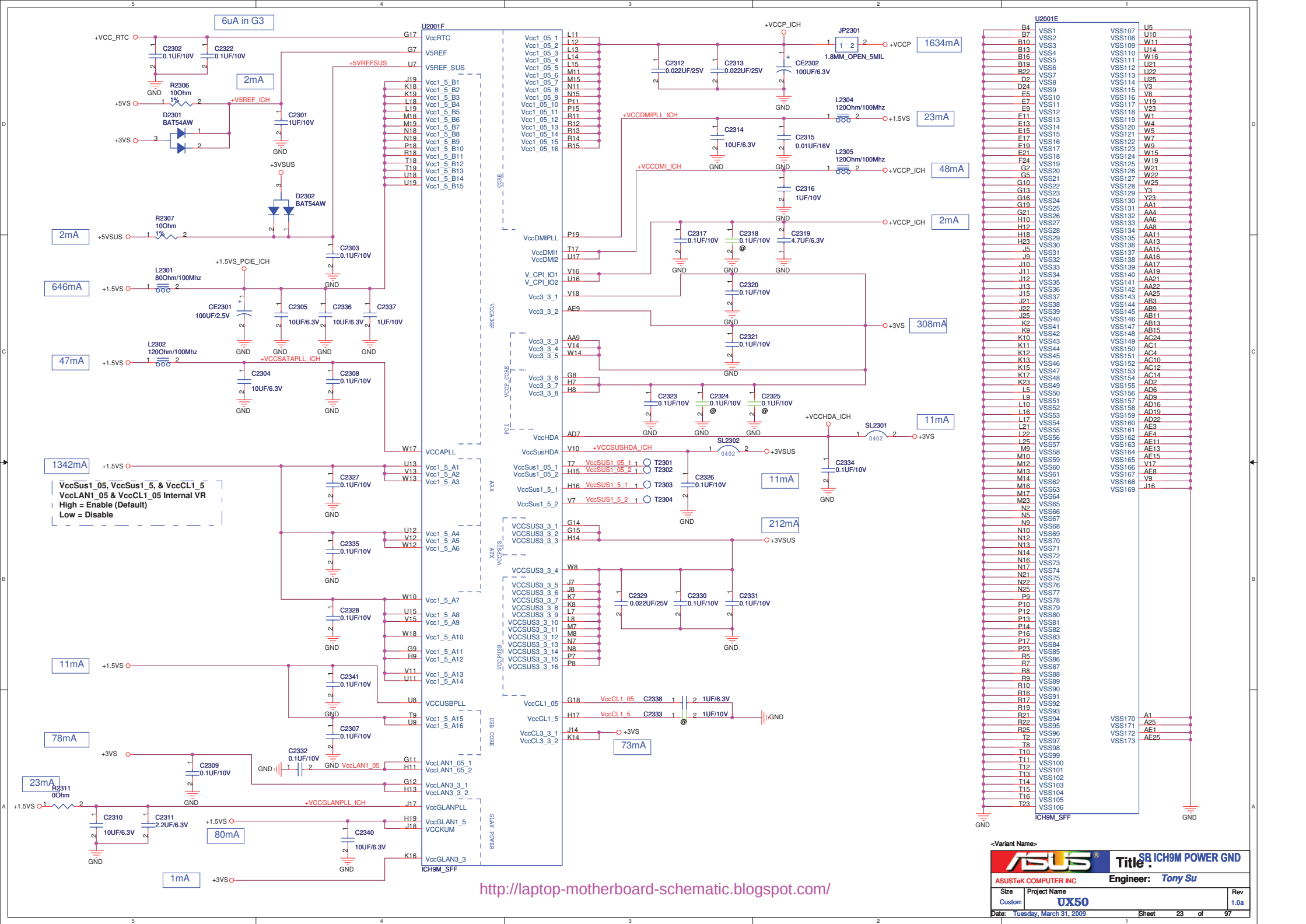
USB

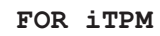
USB

USB

USB





Rev
1.0a



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	25 of 97

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<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	26 of 97



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	27 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

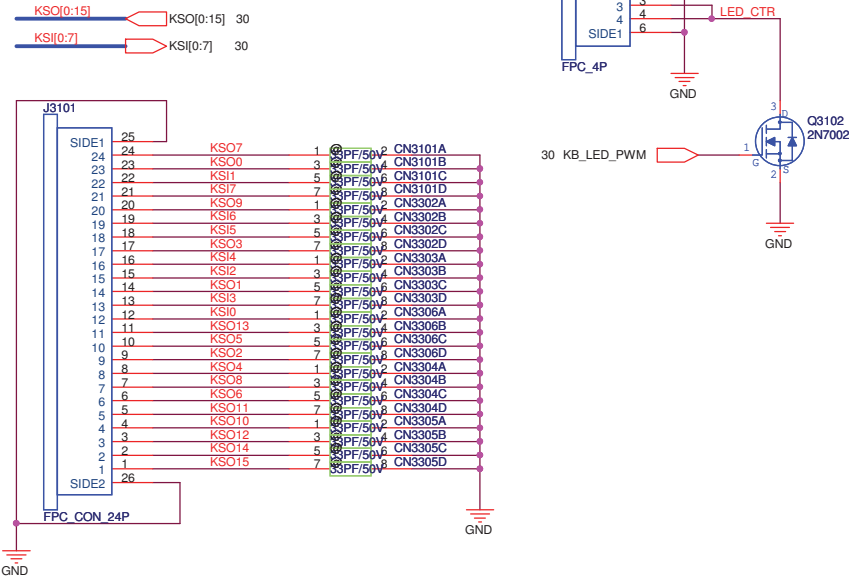


<Variant Name>

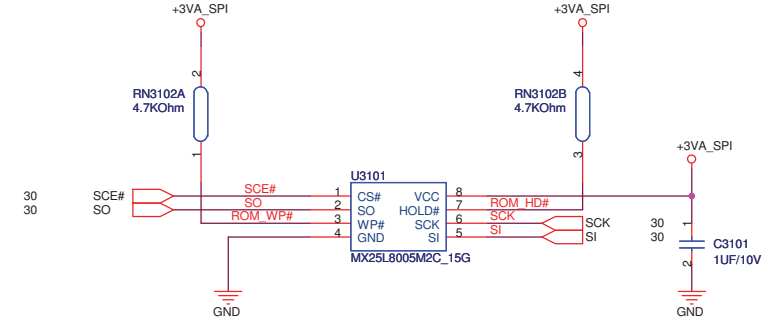
		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	28 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

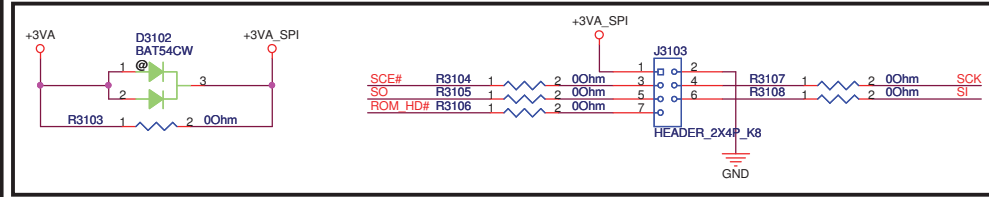
Internal Keyboard



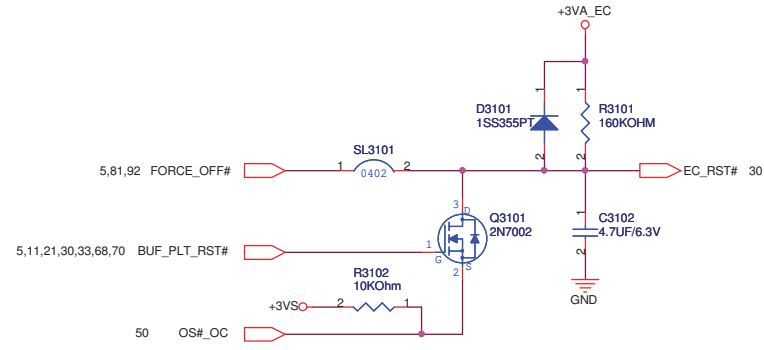
8Mb SPI ROM



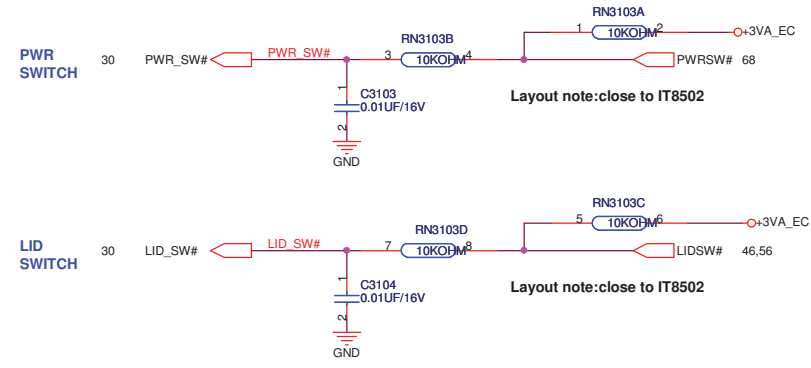
For SPI Flash Debug



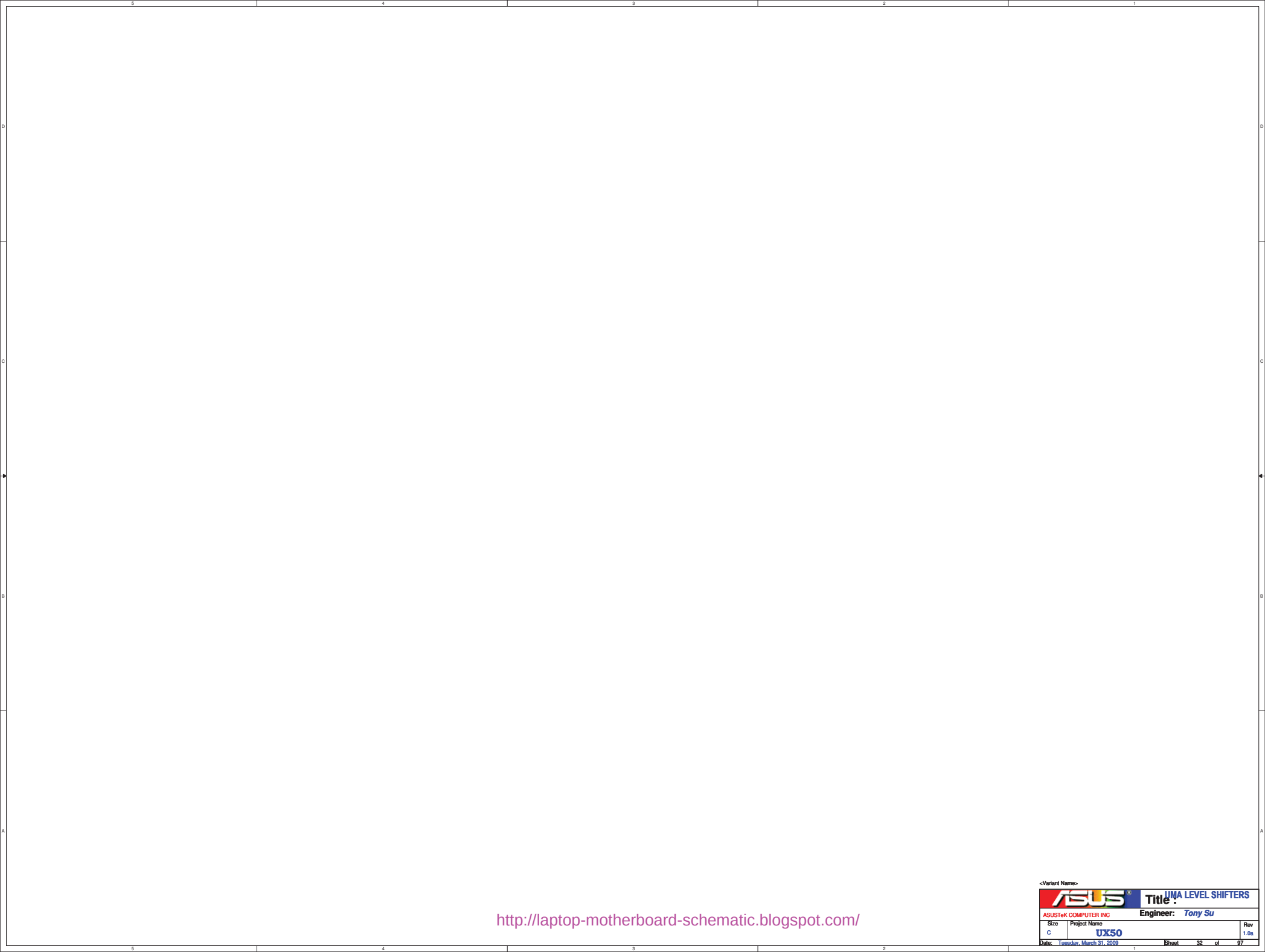
EC RST



For Switch



<http://laptop-motherboard-schematic.blogspot.com/>



<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

**ASUS**

ASUSTeK COMPUTER INC

Size
C

Project Name
UX50

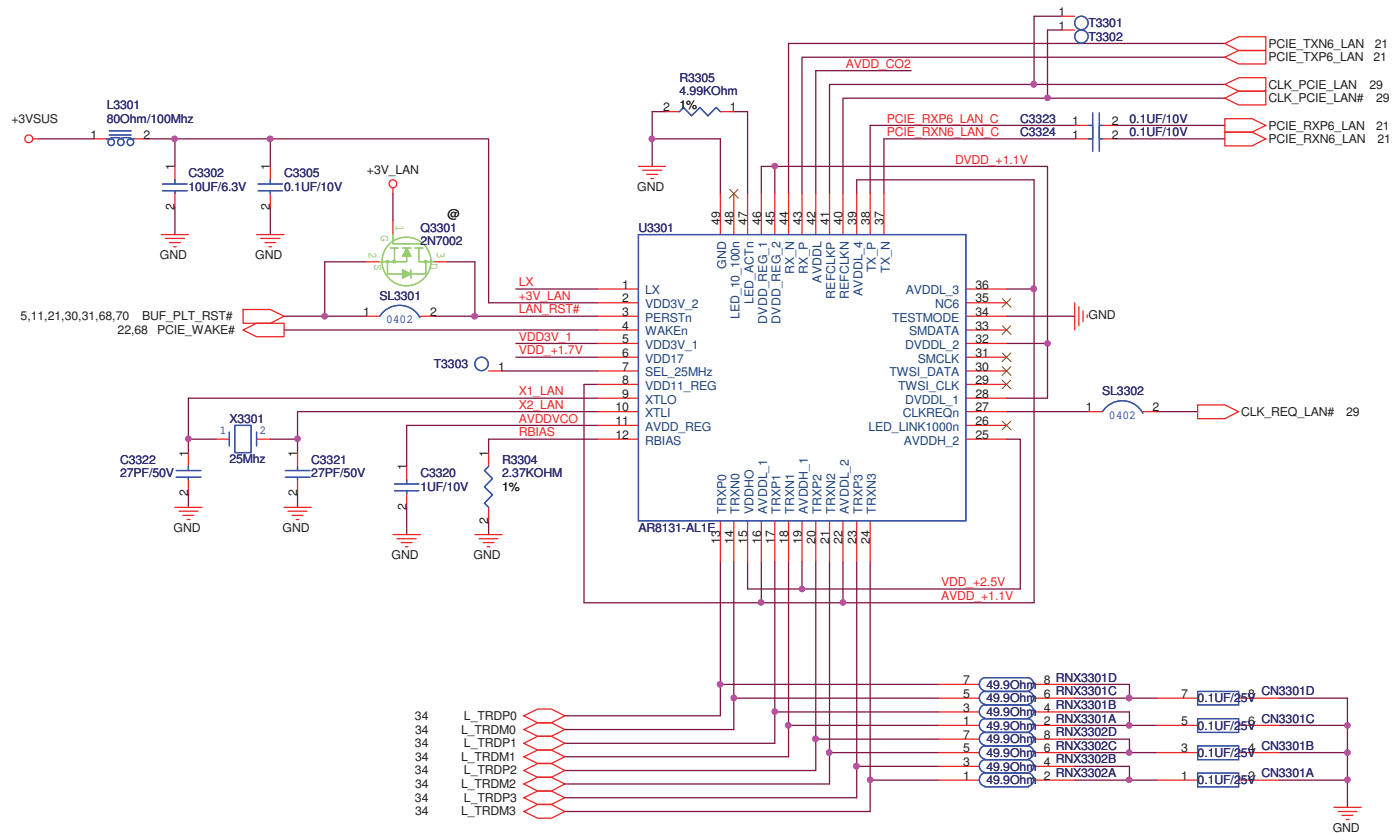
Date: **Tuesday, March 31, 2009**

Title :
UMA LEVEL SHIFTERS

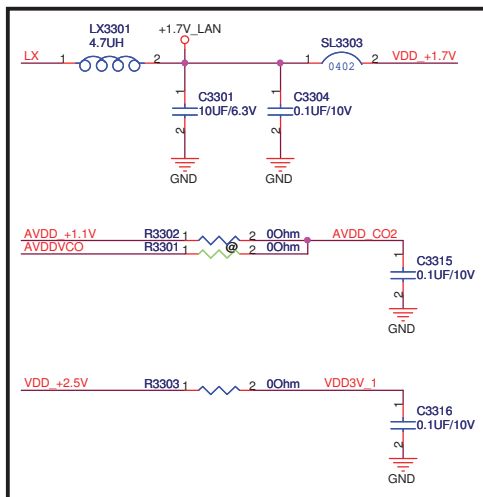
Engineer: **Tony Su**

Rev
1.0a

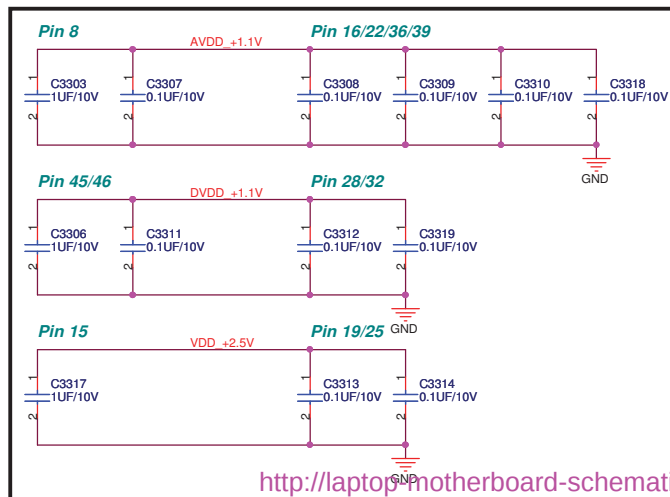
Sheet 32 of 97



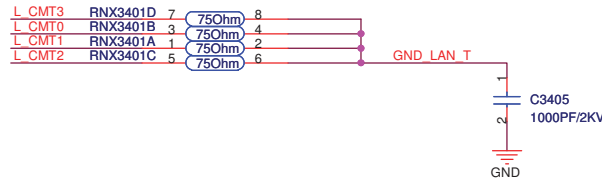
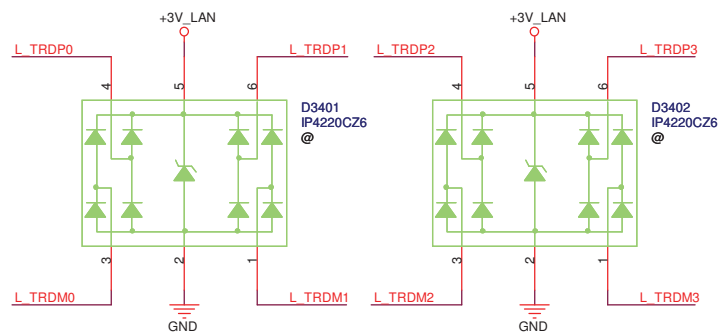
Power



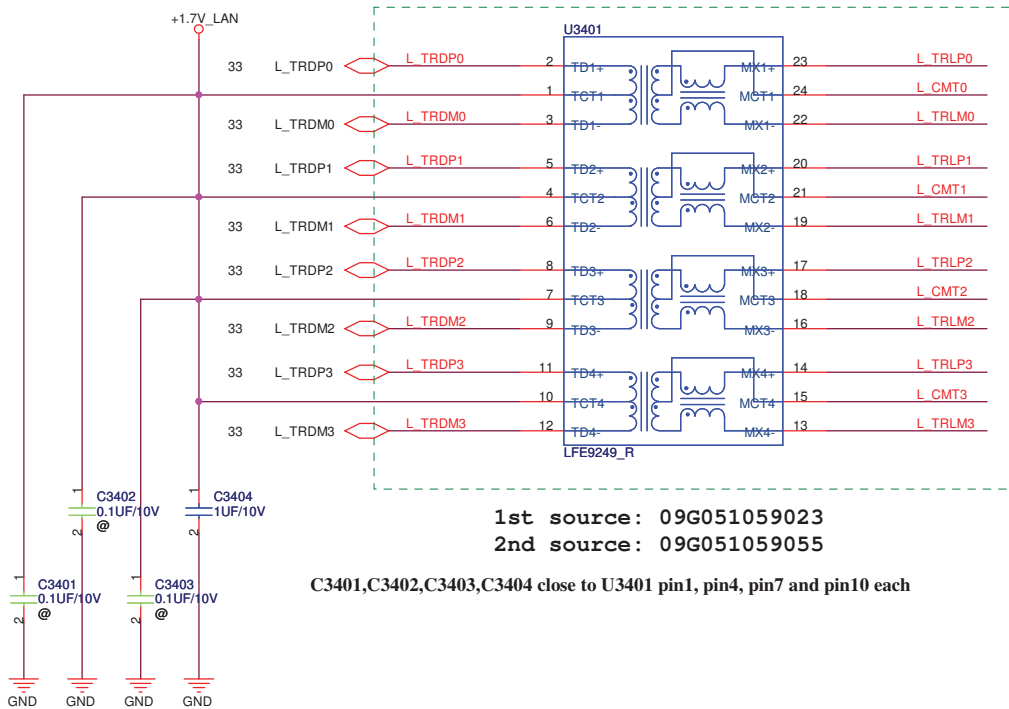
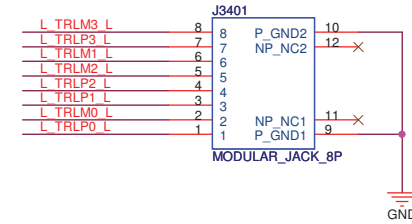
Cap.



<http://laptop-motherboard-schematic.blogspot.com/>

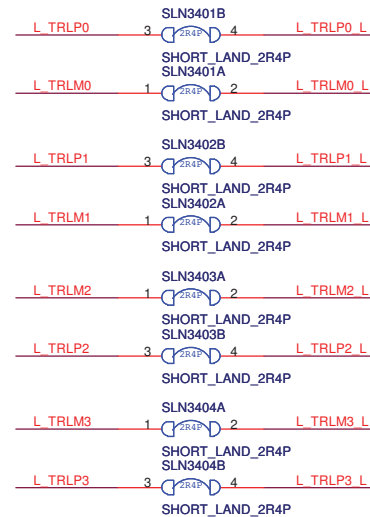


For RJ-45



1st source: 09G051059023
2nd source: 09G051059055

C3401,C3402,C3403,C3404 close to U3401 pin1, pin4, pin7 and pin10 each



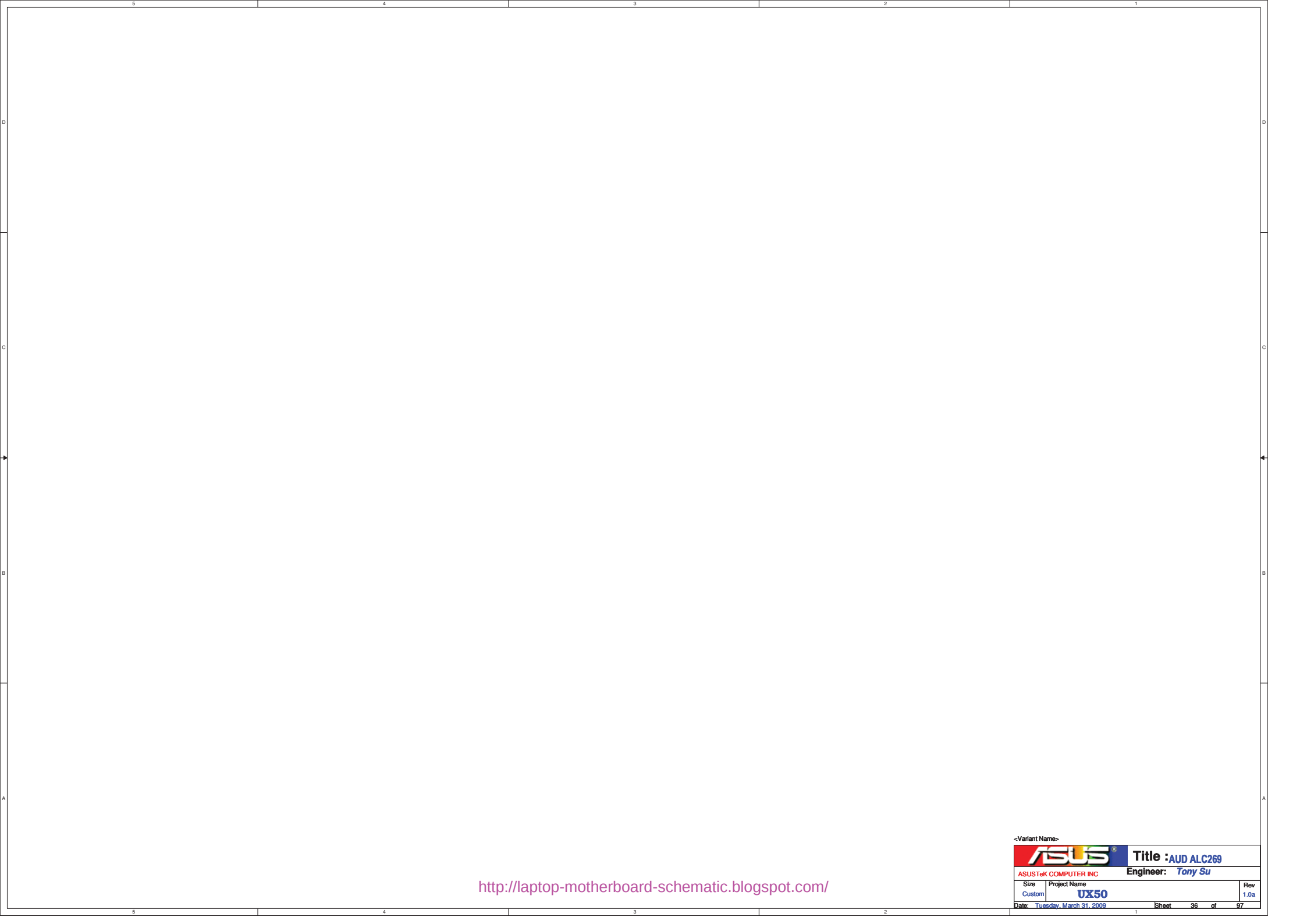
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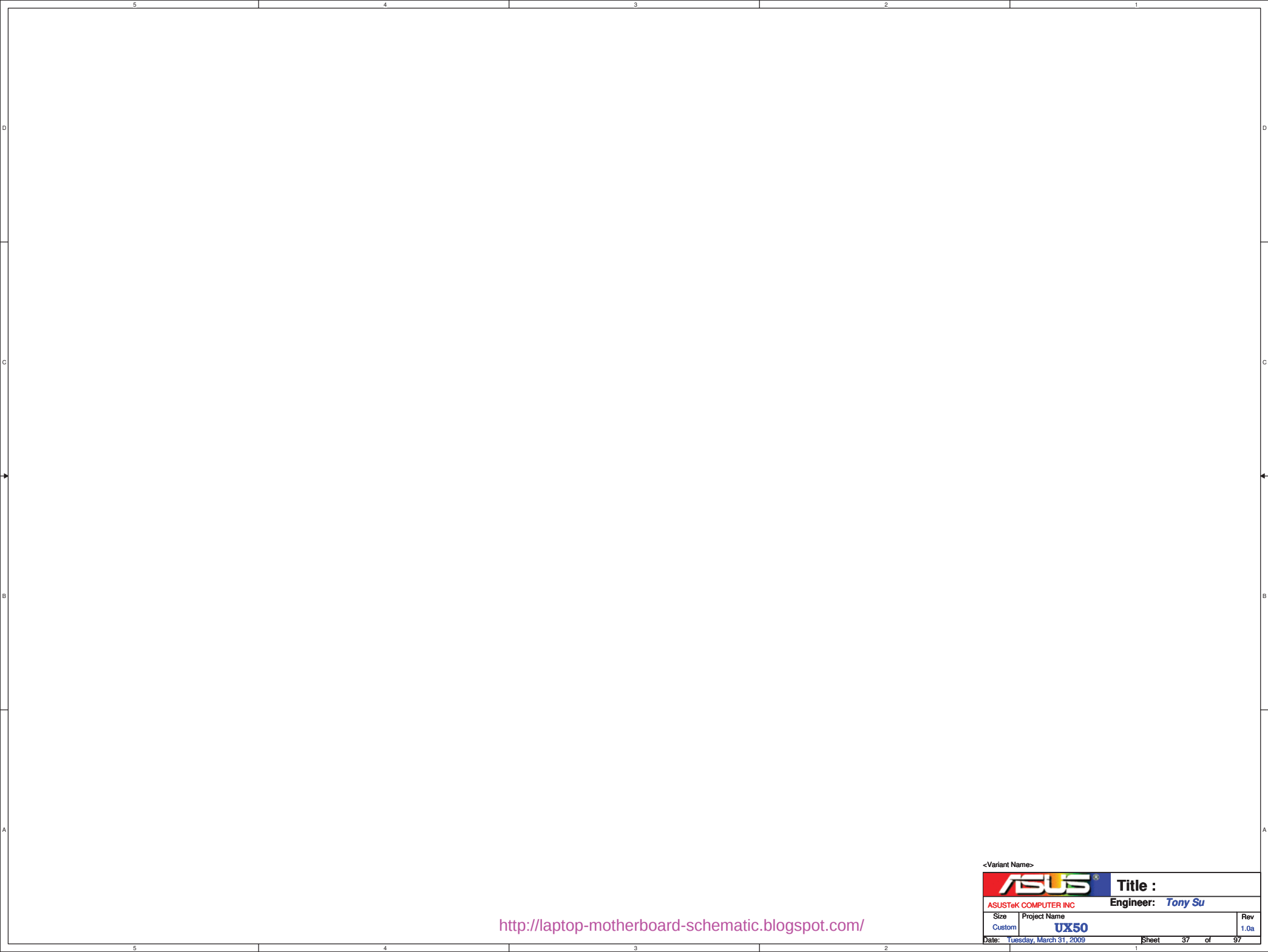
ASUS		Title :LAN RJ45 CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name UX50		Rev 1.0
Date: Tuesday, March 31, 2009		Sheet	34 of 97



<Variant Name>

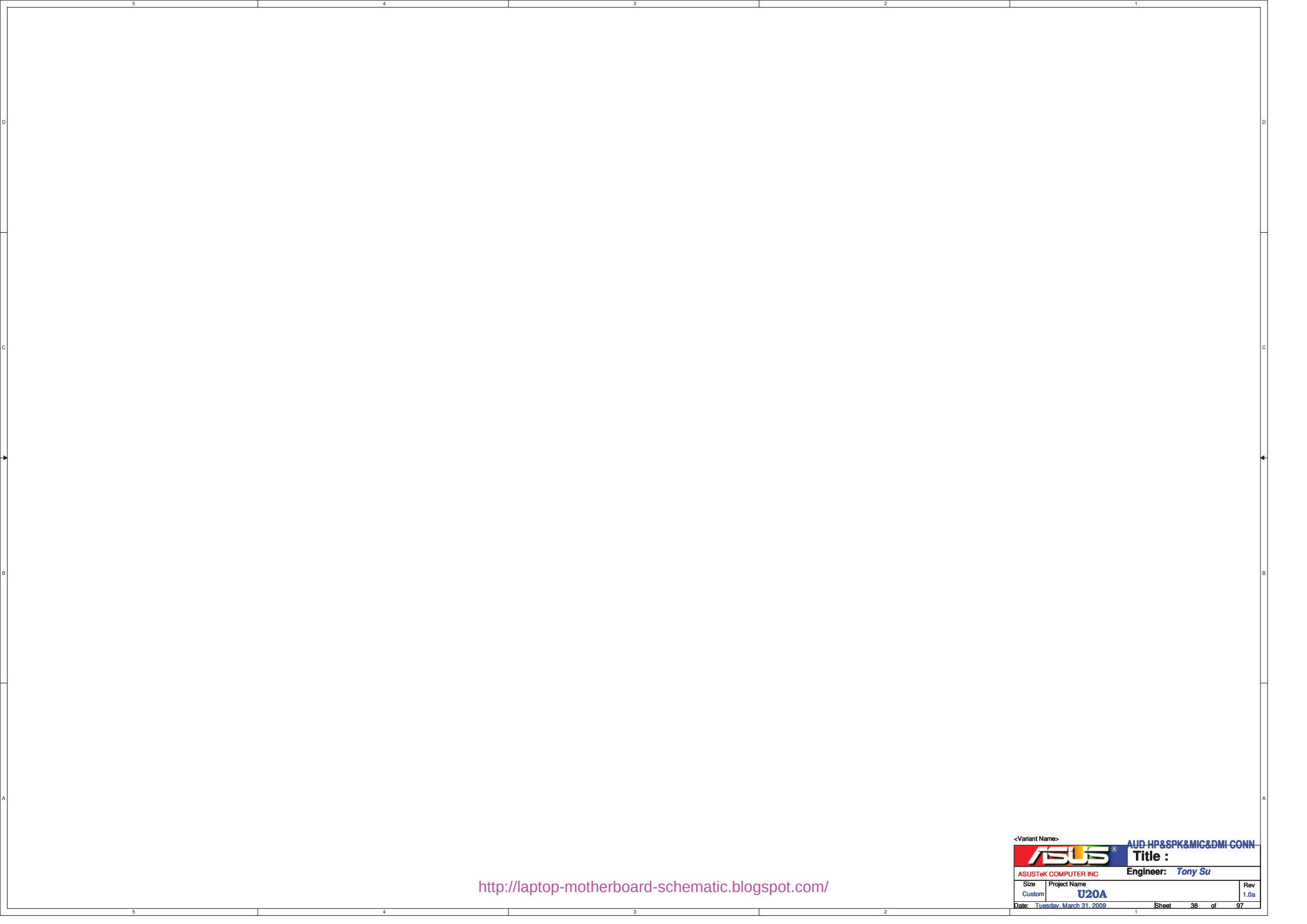
		Title : LAN RJ45 CONN	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name		Rev
A	UX50		1.0
Date: Tuesday, March 31, 2009		Sheet	35 of 97





<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>			
		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name UX50		Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet 37 of 97		1



<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>



AUD HP&SPK&MIC&DMI CONN

ASUSTeK COMPUTER INC

Title :
Engineer: *Tony Su*

Size	Project Name	Rev
Custom	U20A	1.0a

Date: *Tuesday, March 31, 2009* Sheet 38 of 97



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: Tuesday, March 31, 2009		Sheet	39 of 97

<http://laptop-motherboard-schematic.blogspot.com/>



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	40 of 97

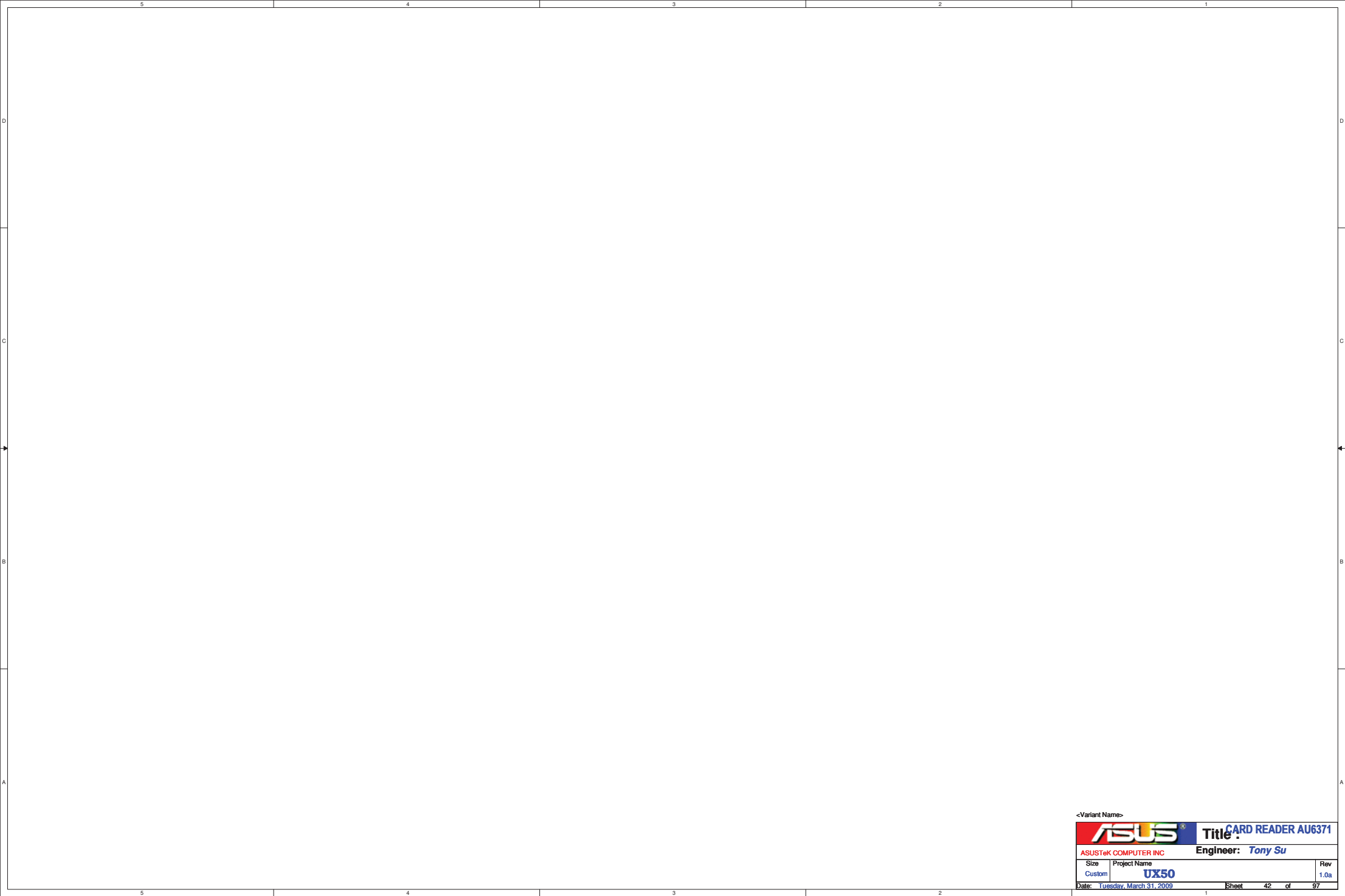
<http://laptop-motherboard-schematic.blogspot.com/>



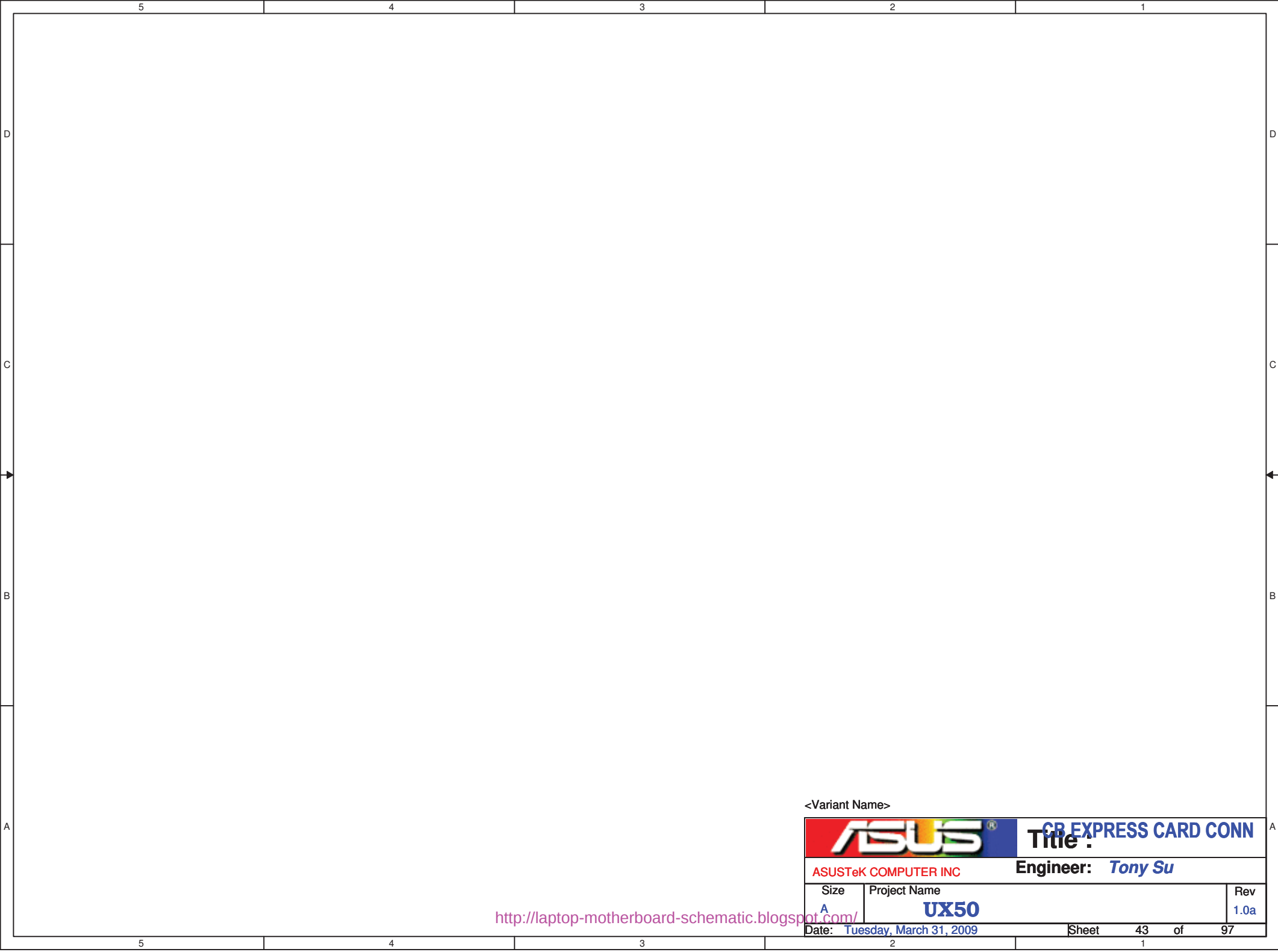
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	41 of 97

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<Variant Name>			
		Title: CARD READER AU6371	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name		Rev
Custom	UX50		1.0a
Date: Tuesday, March 31, 2009	Sheet 42 of 97		

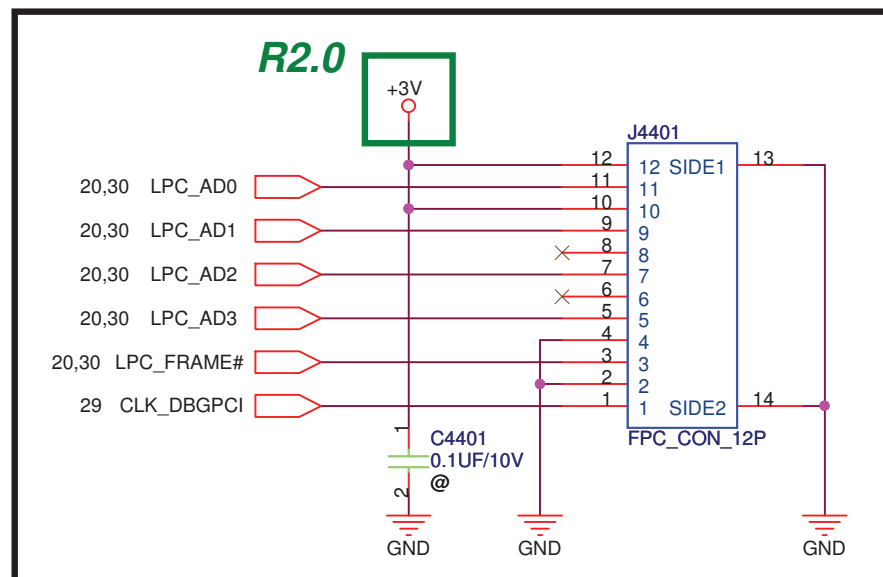


<Variant Name>

		Title : CB EXPRESS CARD CONN	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size A	Project Name UX50		Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet	43 of 97

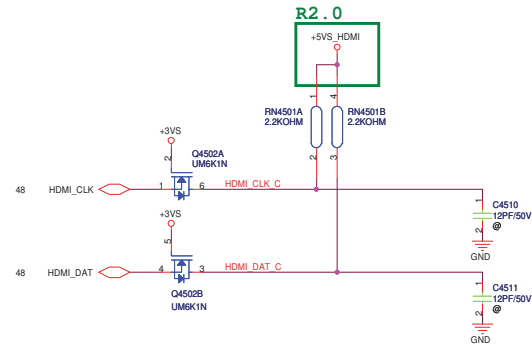
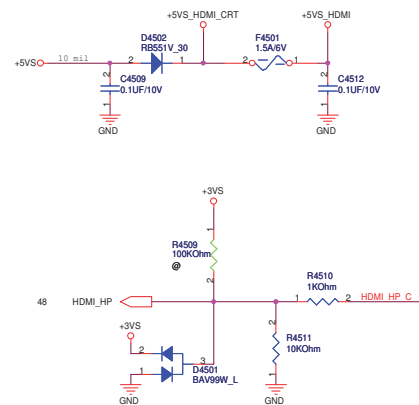
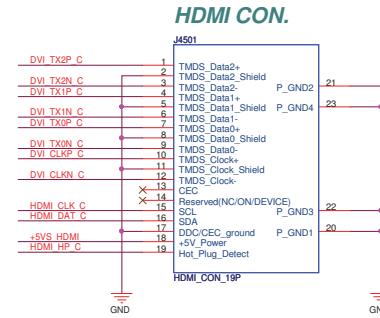
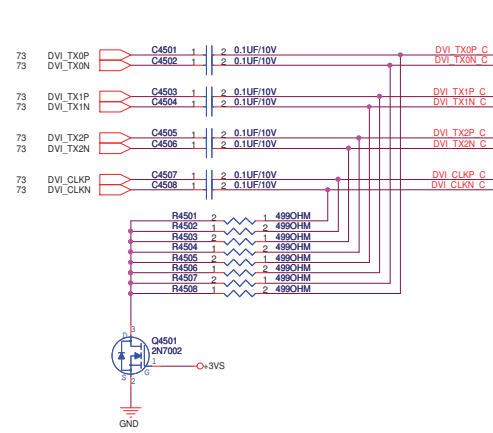
<http://laptop-motherboard-schematic.blogspot.com/>

LPC DEBUG PORT

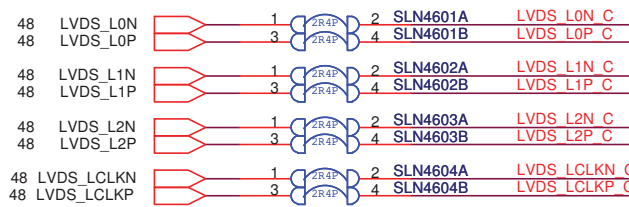
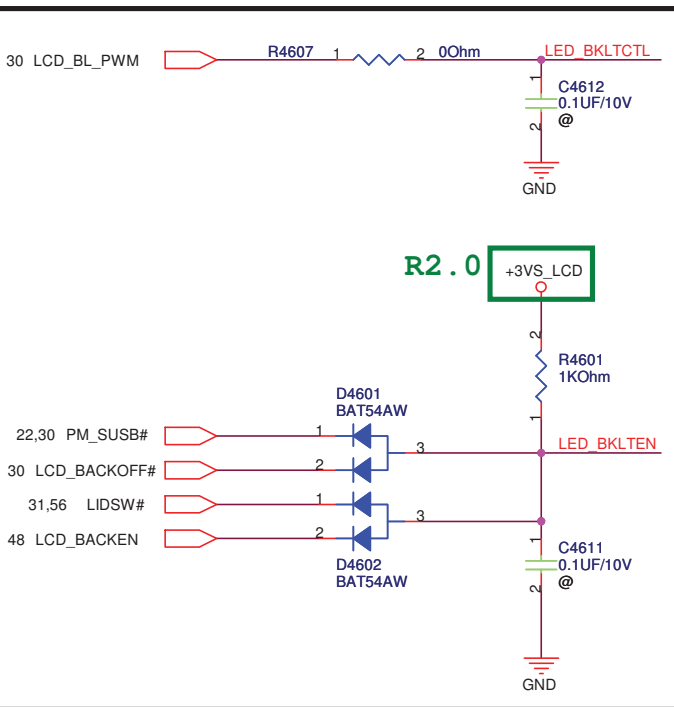
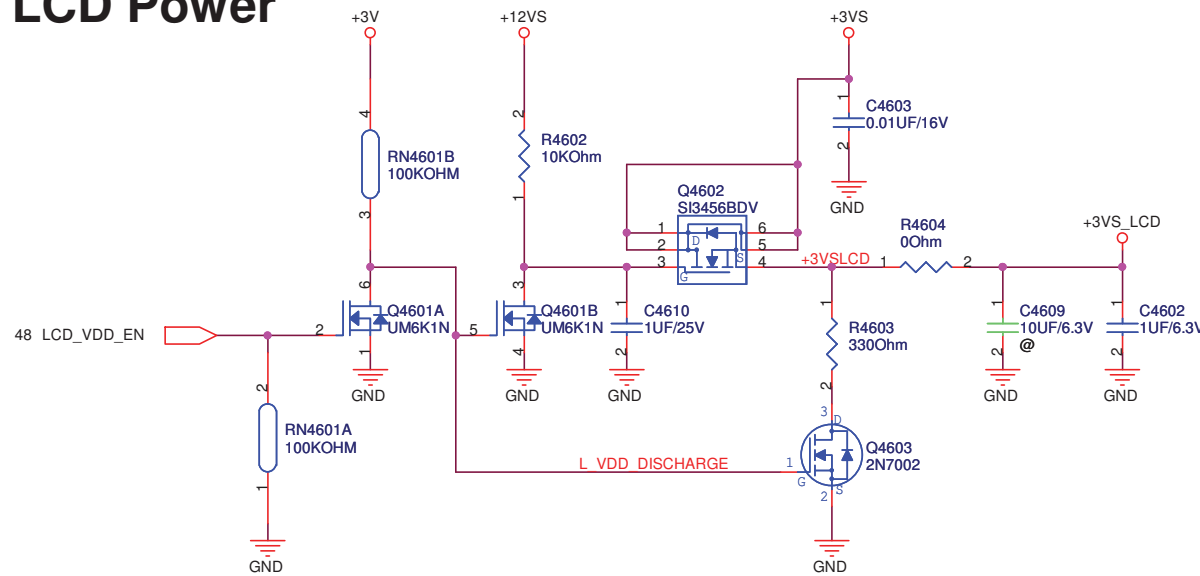


<Variant Name>

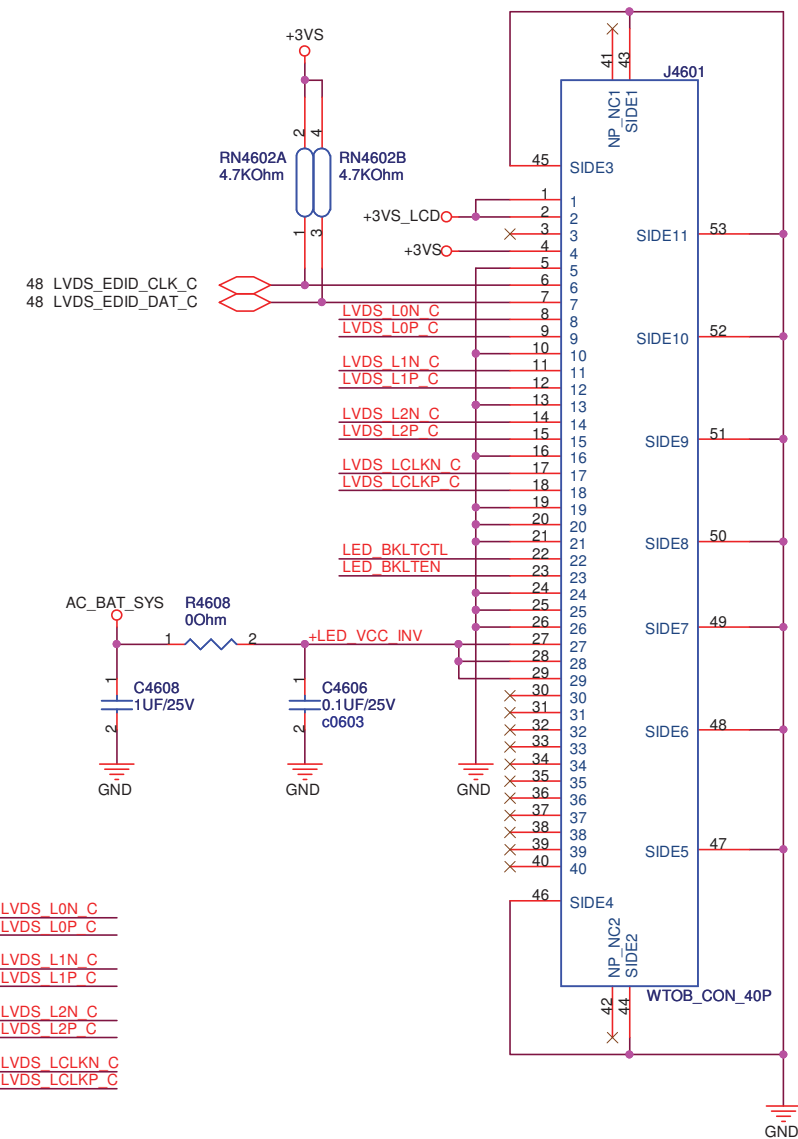
ASUS		Title :BUG DEBUG PORT	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
A	UX50	1.0a	
Date: Tuesday, March 31, 2009		Sheet	44 of 97



LCD Power



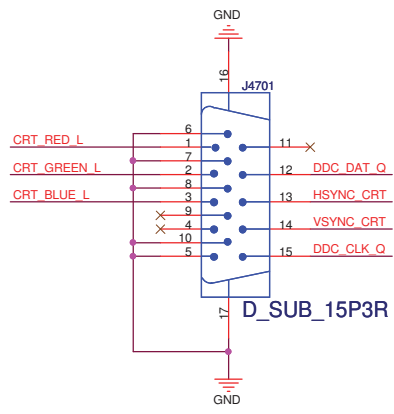
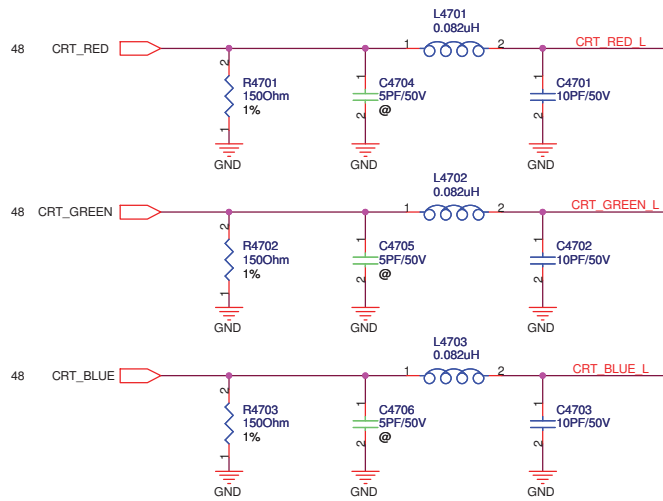
LVDS CONN



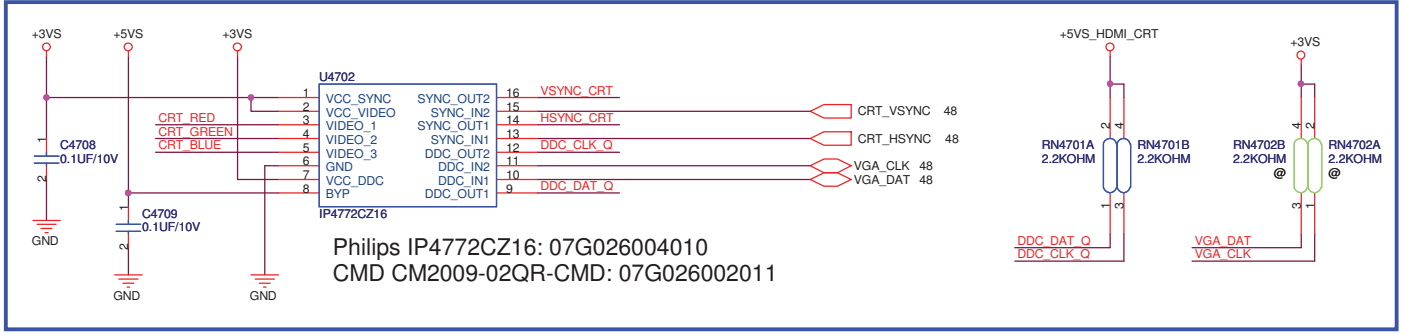
<Variant Name>

ASUS		Title :CRT LVDS CONN	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size Custom	Project Name UX50	Rev 1.0a	
Date: Tuesday, March 31, 2009		Sheet	46 of 97

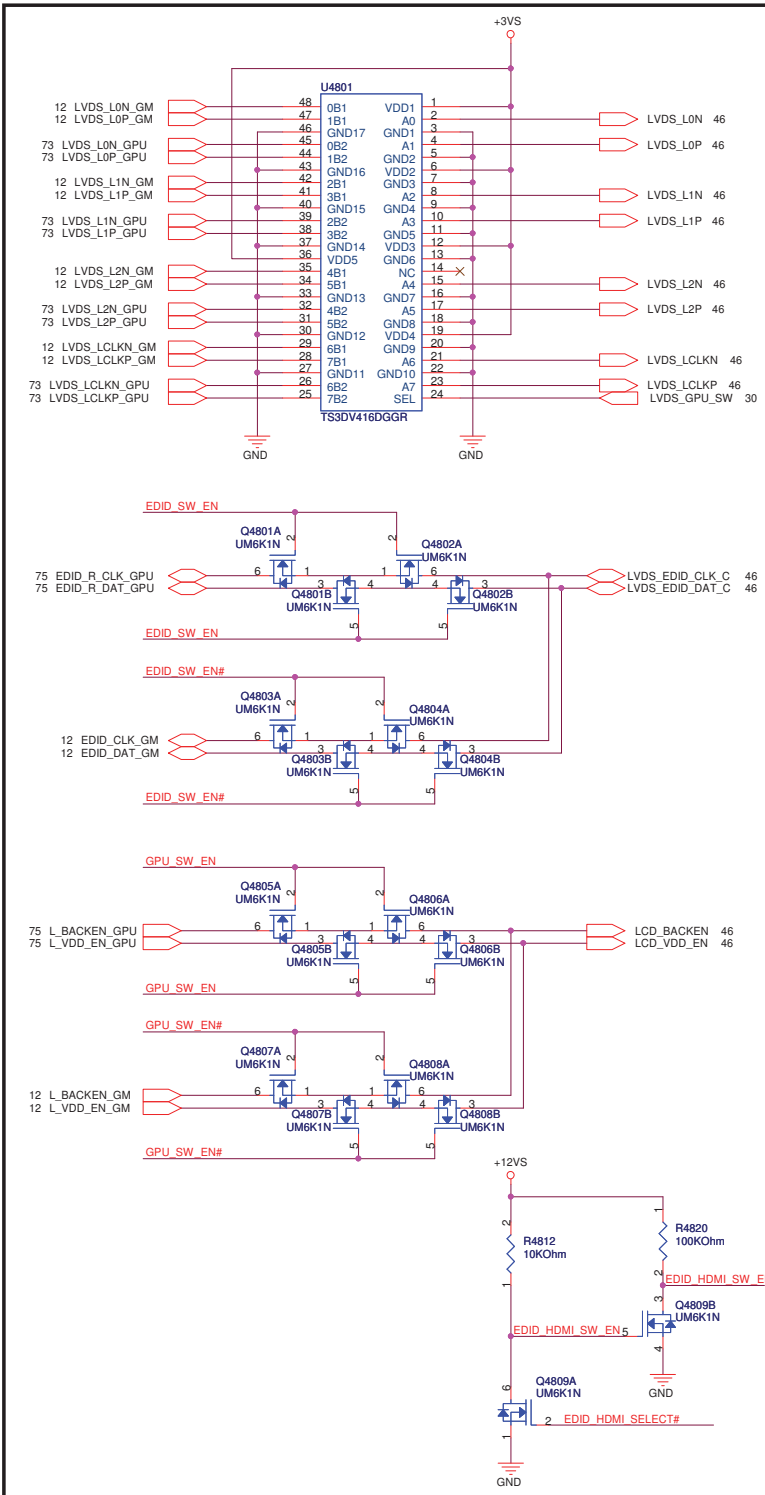
CRT Connector



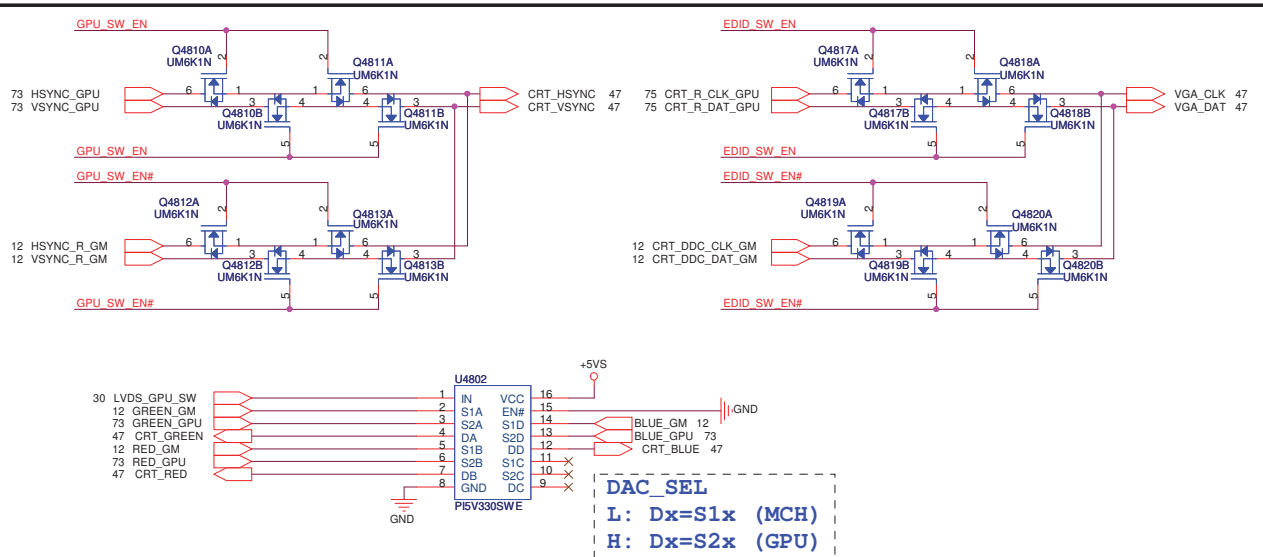
PLACE ESD IC near J4701



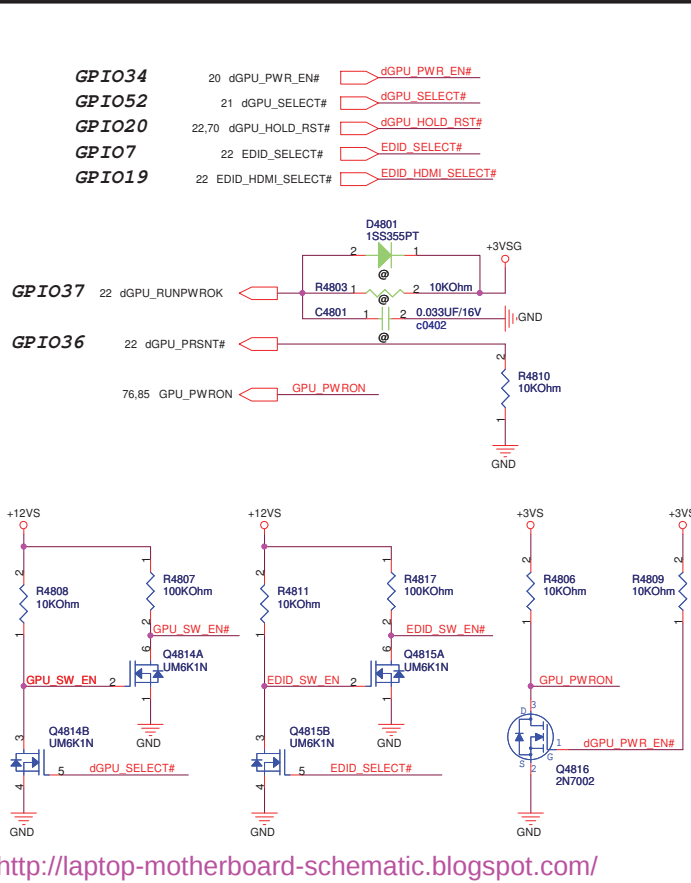
LVDS Switch



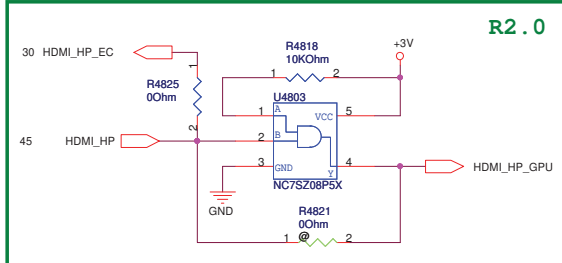
CRT Switch



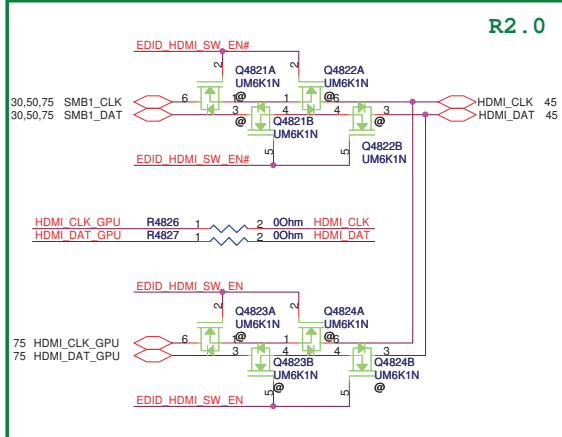
Control Signal from ICH9M

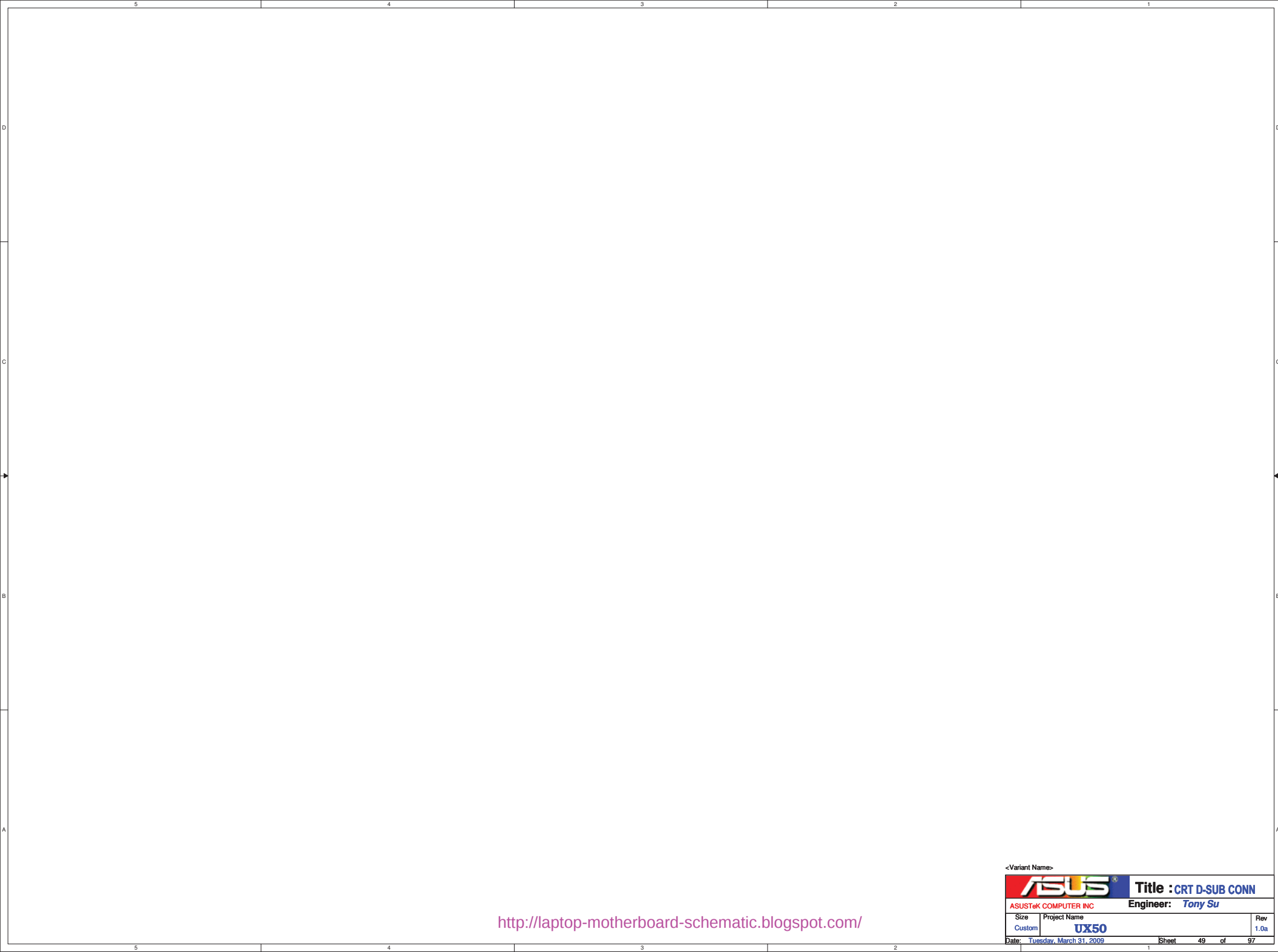


HDMI Hot-Plug Detect Switch



HDMI I2C Switch





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<Variant Name>

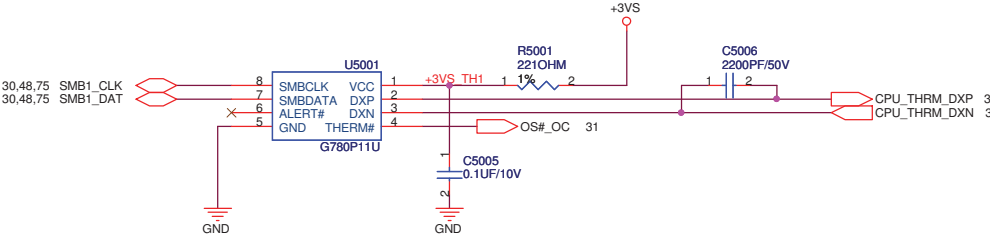
**ASUSTeK COMPUTER INC**

Title : CRT D-SUB CONN
Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 **Sheet** 49 **of** 97

Thermal Seneor



1nd: 06G023096010 G780P11U SOP-8
2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and
MEM_THERM_DA , MEM_THERM_DC on
the same layer

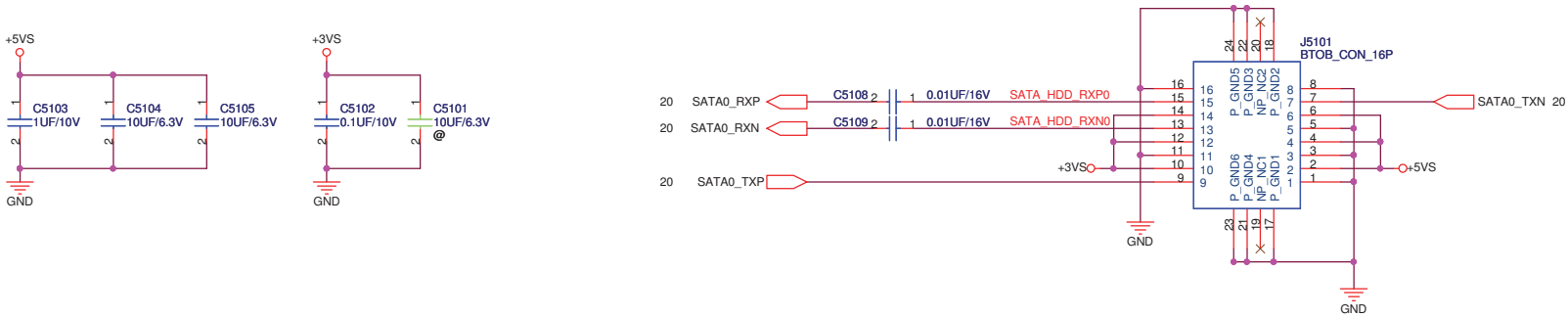
-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power

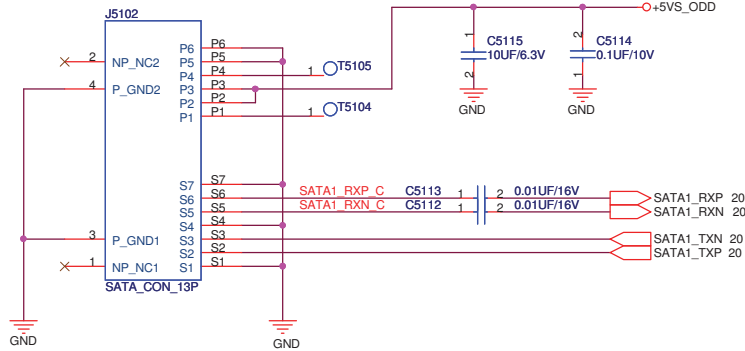
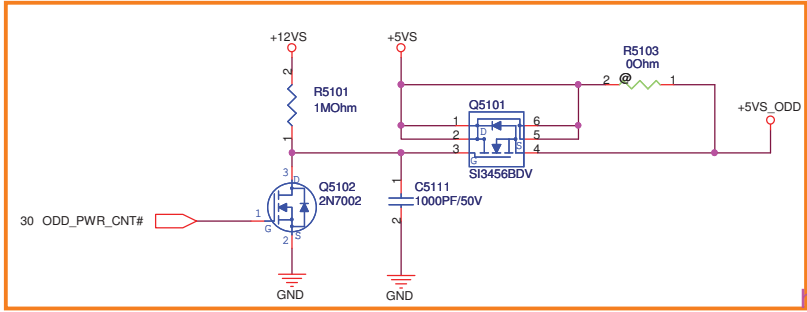
<Variant Name> FAN THERMAL SENSOR FAN CONN

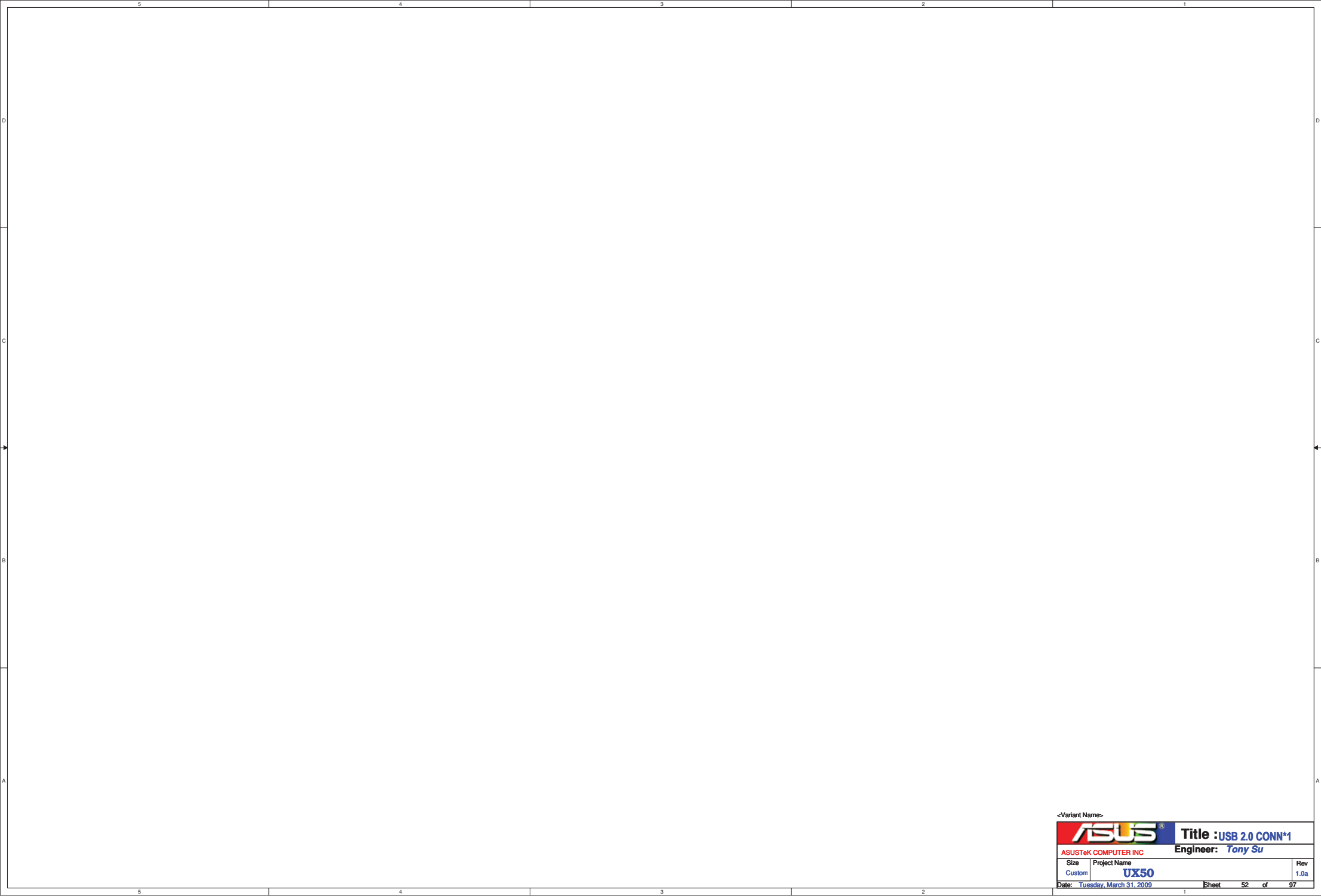
ASUS		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name UX50	Date: Tuesday, March 31, 2009	Rev 1.0a
Sheet 50 of 97			

SATA HDD



SATA ODD





<Variant Name>

		Title :USB 2.0 CONN*1	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name UX50		Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet	52 of 97



<http://laptop-motherboard-schematic.blogspot.com/>

		Title : PCI_Minicard	
ASUSTeK COMPUTER INC. NB1		Engineer: Tony Su	
Size	Project Name		Rev
Custom	UX50		1.00
Date: Tuesday, March 31, 2009		Sheet	53 of 97



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	54 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

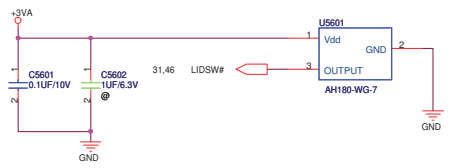


<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: Tuesday, March 31, 2009		Sheet	55 of 97

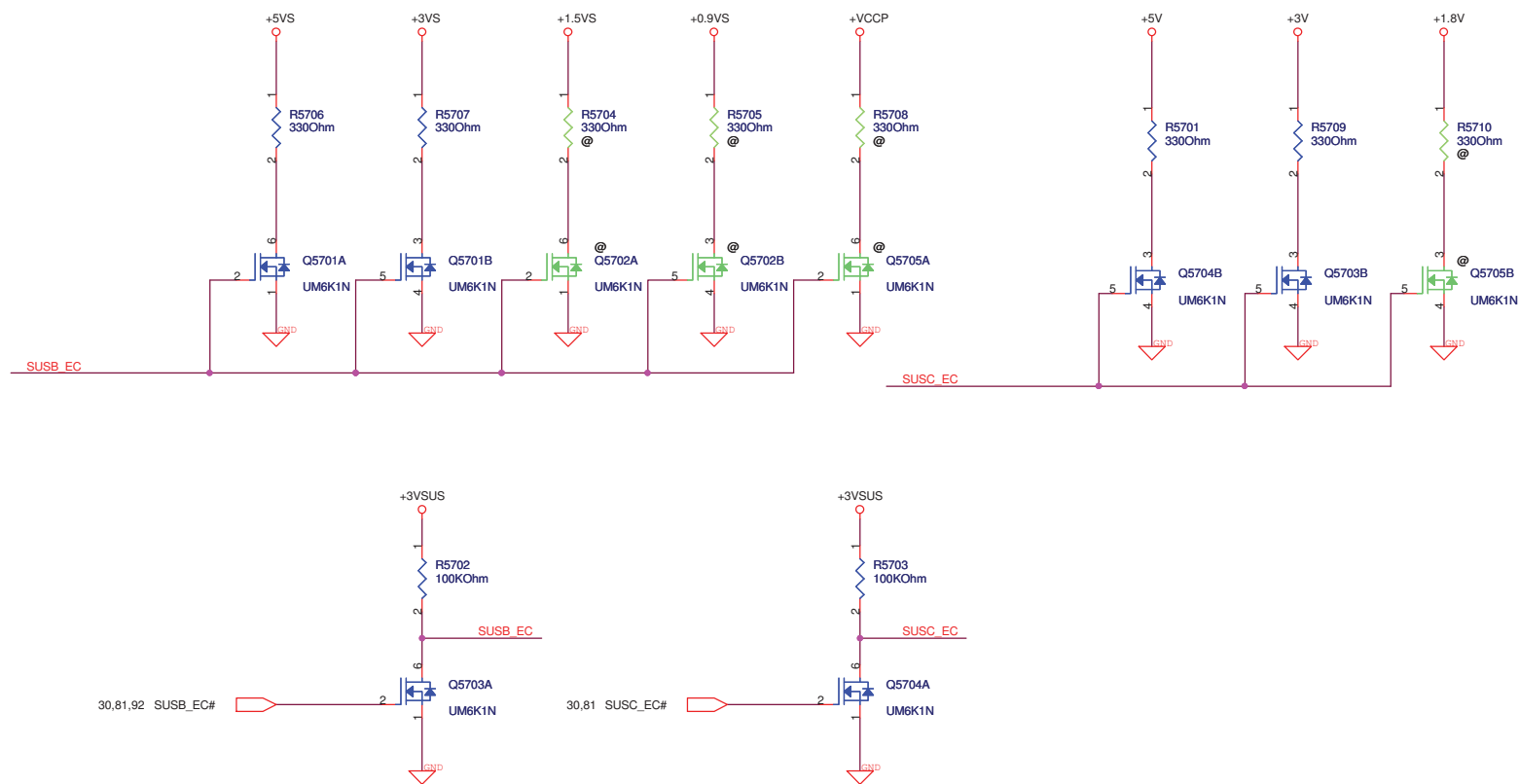
<http://laptop-motherboard-schematic.blogspot.com/>

LID SENSER



Hall Sensor Second Source
06G036012010 Cheap
06G036013010
06G036009011
06G051001012

Discharge Circuit



<http://laptop-motherboard-schematic.blogspot.com/>



<Variant Name>

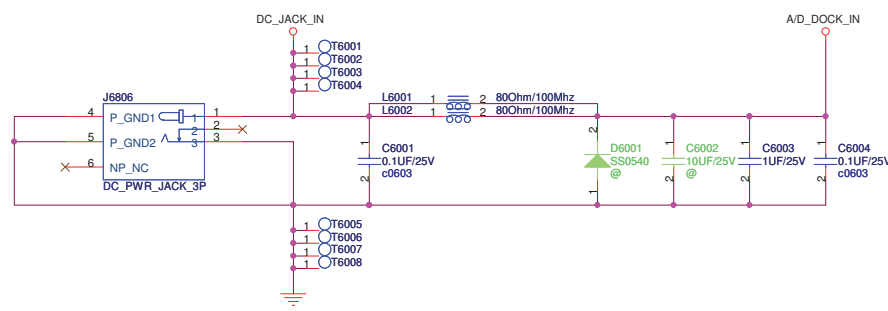
		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	58 of 97

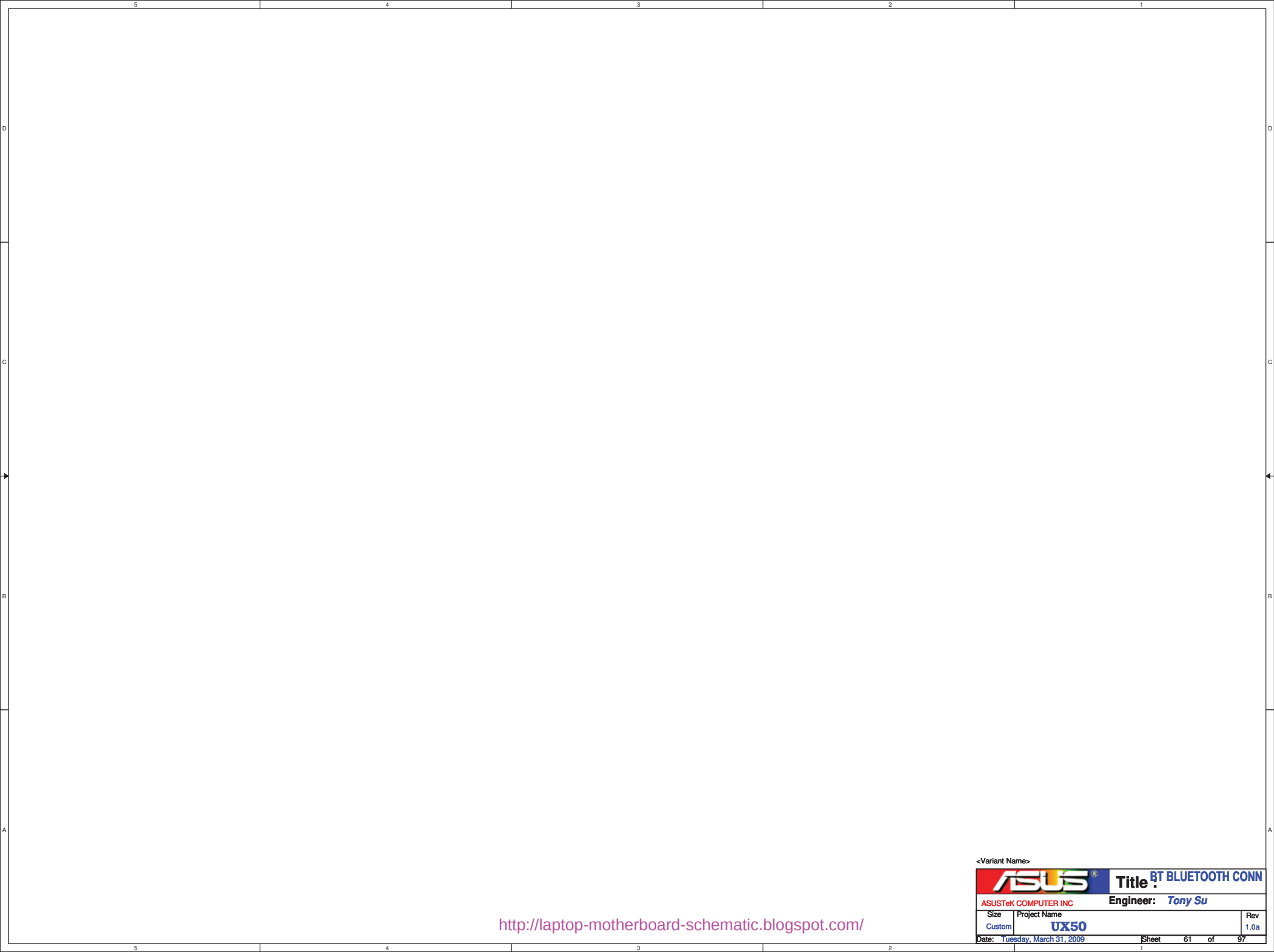


<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	59 of 97

<http://laptop-motherboard-schematic.blogspot.com/>





<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

**ASUS**[®]

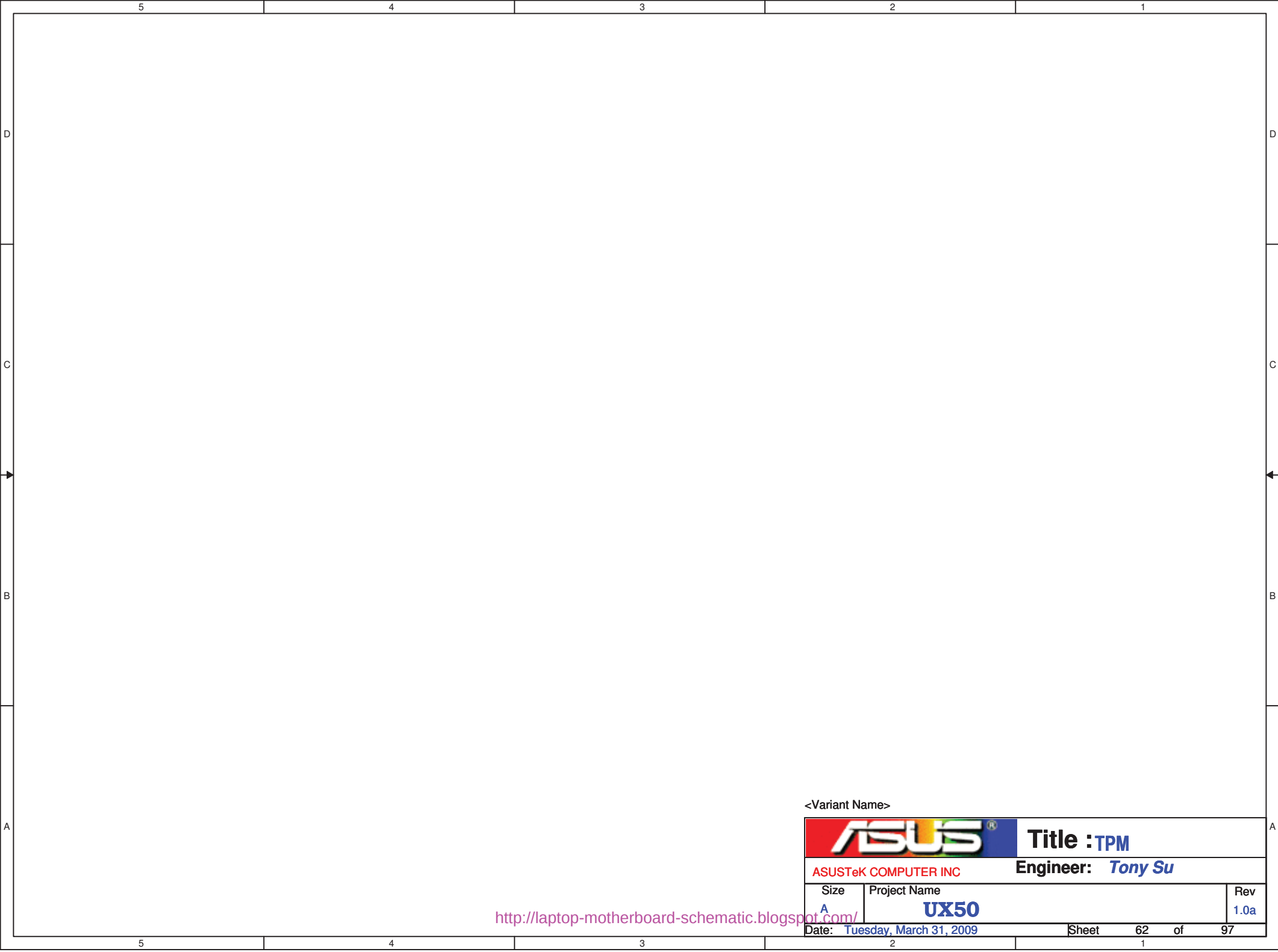
Title : BT BLUETOOTH CONN

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009Sheet 61 of 97



<Variant Name>

		Title : TPM	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: Tuesday, March 31, 2009		Sheet	62 of 97



<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	63 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

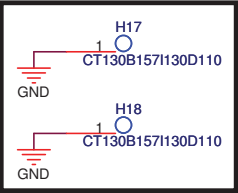
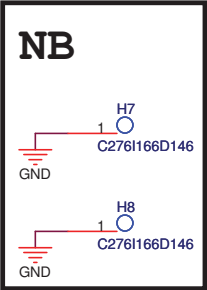
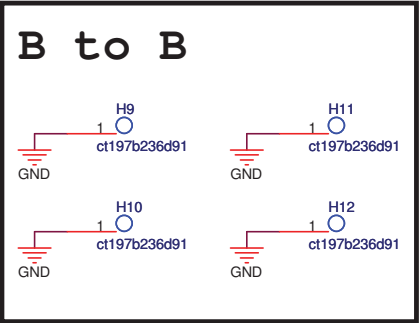
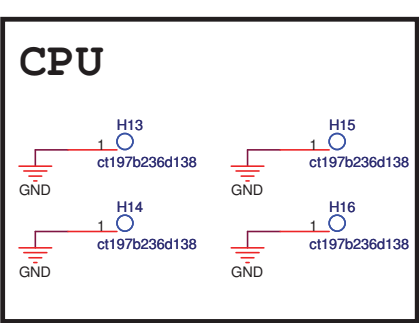
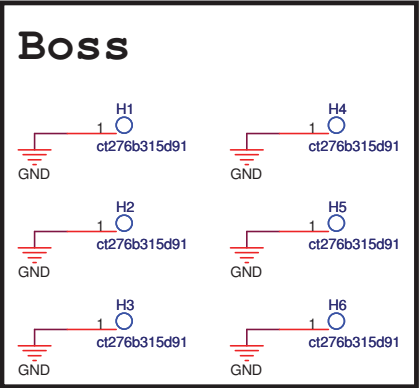


<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	64 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

Screw Hole & SMT Nut



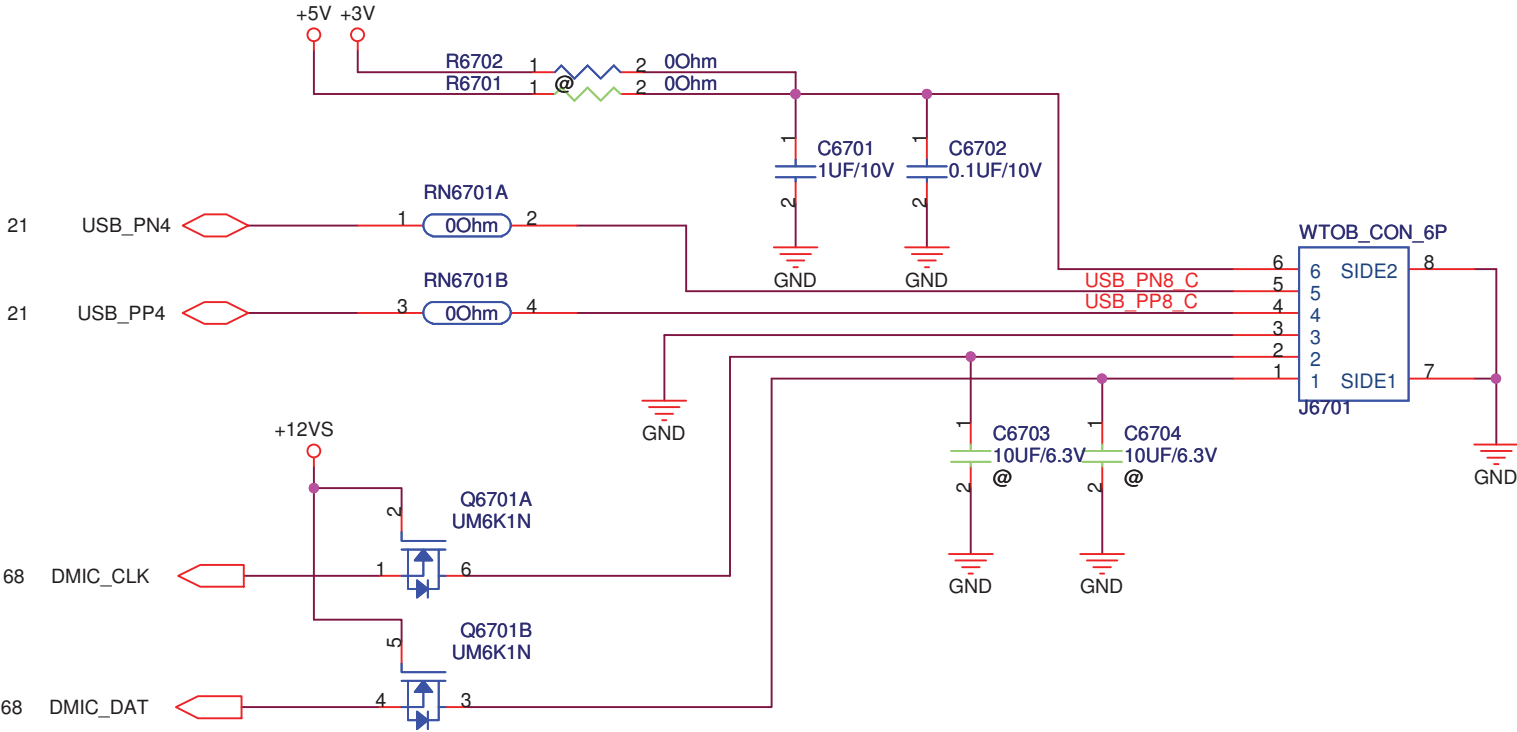


<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: <i>Tuesday, March 31, 2009</i>		Sheet	66 of 97

<http://laptop-motherboard-schematic.blogspot.com/>

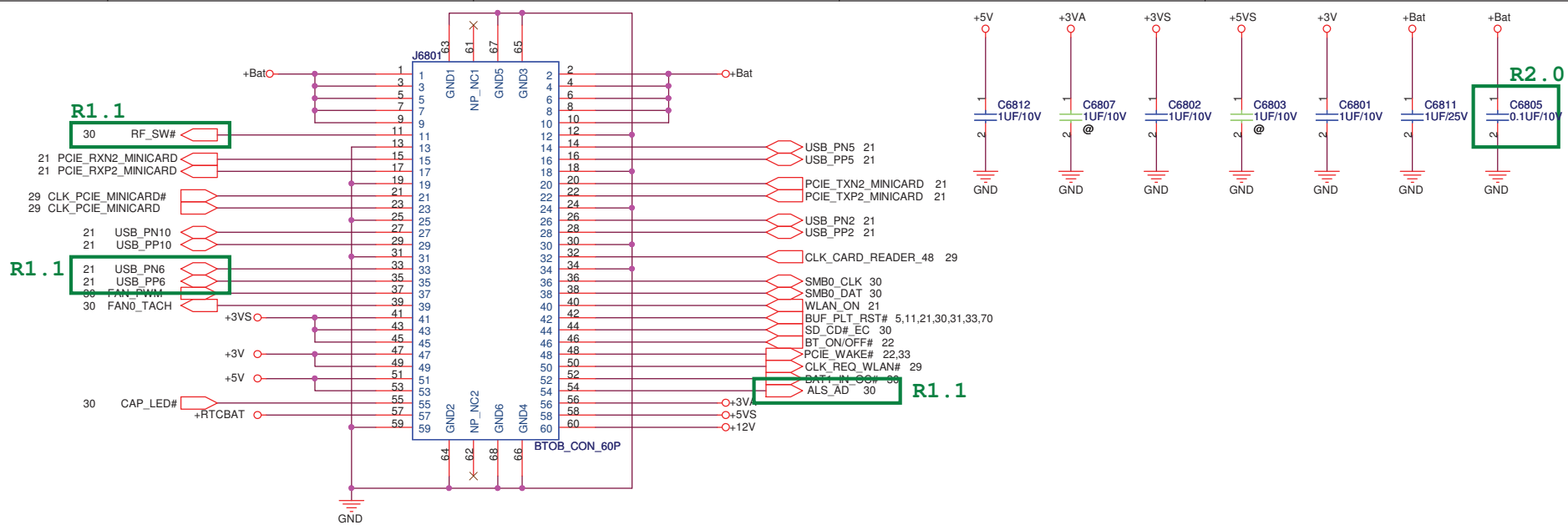
Camera Module



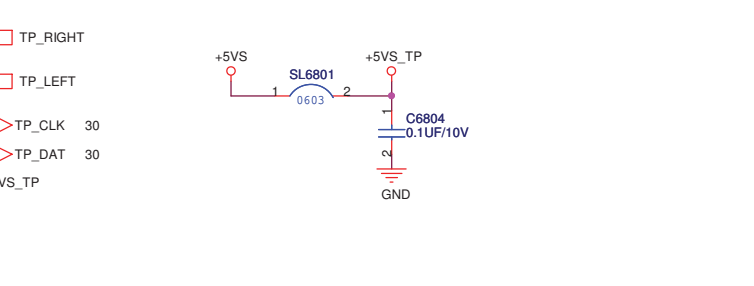
<Variant Name>

		Title : CMOS CAMERA	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name		Rev
A	UX50		1.0a
Date: Tuesday, March 31, 2009		Sheet	67 of 97

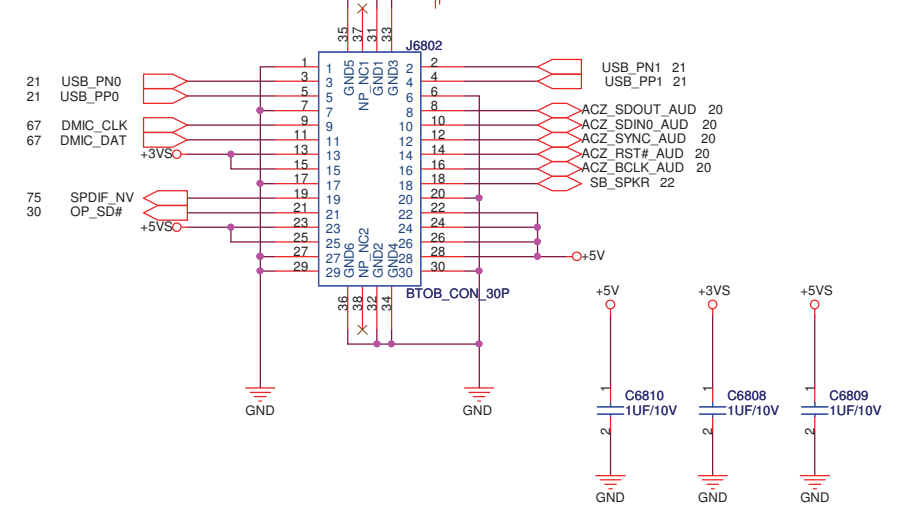
CR Board



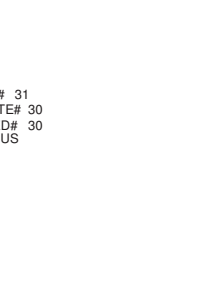
Touch Pad Board



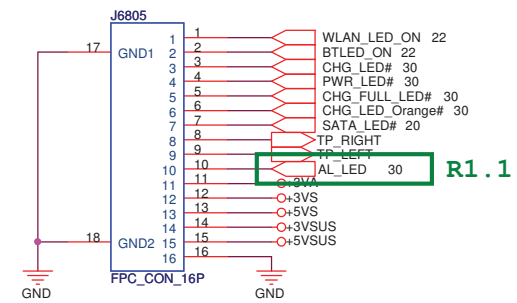
Audio Board



Switch Board



LED Board



<Variant Name>

ASUS		Title : B TO B CONN	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size B	Project Name UX50	Rev 1.0a	
Date: Tuesday, March 31, 2009		Sheet 68 of 97	

SYSTEM

+VCCP   +VCCP 3,4,5,10,11,12,14,15,20,23,29,57,76,82

+VCC_GMCH   +VCC_GMCH 14

+VGFX_CORE   +VGFX_CORE 14

+3VS   +3VS 7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92

+VCORE   +VCORE 4,5,80

+1.5VS   +1.5VS 4,15,20,23,57,84

+12VS   +12VS 22,46,48,51,67,91

AC_BAT_SYS   AC_BAT_SYS 46,80,81,82,83,85,86,88

+5V   +5V 31,57,67,68,91

+5VS   +5VS 23,45,47,48,51,57,68,80,84,91

+3VA   +3VA 20,30,31,56,68,81,88

+VCC_RTC   +VCC_RTC 20,23

+3V   +3V 44,46,48,57,67,68,70,91

+3VSUS   +3VSUS 20,21,22,23,30,33,57,68,76,81,85,91,92

+5VSUS   +5VSUS 23,68,80,81,82,83,85,86,88,91

+3VPLL   +3VPLL 30

+3VACC   +3VACC 30

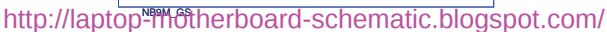
+3VA_ECO   +3VA_EC 30,31

+5VA   +5VA 81

+12V   +12V 68,91

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		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		1.0a
Date: Tuesday, March 31, 2009		Sheet 69 of 97	



72 FBAD[0..63]
72 FBADQM[0..7]
72 FBAWDS[0..7]
72 FBARDQS[0..7]

U7001B
2/13 FRAME BUFFER

FBA_D0 D21
FBA_D1 D22
FBA_D2 B22
FBA_D3 A22
FBA_D4 C24
FBA_D5 B25
FBA_D6 A25
FBA_D7 A26
FBA_D8 D22
FBA_D9 E24
FBA_D10 E24
FBA_D11 D24
FBA_D12 D26
FBA_D13 E24
FBA_D14 D27
FBA_D15 B27
FBA_D16 D16
FBA_D17 E16
FBA_D18 D17
FBA_D19 F18
FBA_D20 D20
FBA_D21 F20
FBA_D22 E21
FBA_D23 F21
FBA_D24 C16
FBA_D25 B18
FBA_D26 C18
FBA_D27 D18
FBA_D28 C19
FBA_D29 C21
FBA_D30 B21
FBA_D31 A21
FBA_D32 P22
FBA_D33 P24
FBA_D34 R23
FBA_D35 R24
FBA_D36 T23
FBA_D37 U24
FBA_D38 V23
FBA_D39 V24
FBA_D40 N25
FBA_D41 N26
FBA_D42 R25
FBA_D43 R26
FBA_D44 T25
FBA_D45 V26
FBA_D46 V25
FBA_D47 V27
FBA_D48 W22
FBA_D49 W22
FBA_D50 W23
FBA_D51 W24
FBA_D52 A25
FBA_D53 AB23
FBA_D54 AB24
FBA_D55 AC24
FBA_D56 W25
FBA_D57 W26
FBA_D58 W27
FBA_D59 A26
FBA_D60 AB25
FBA_D61 AB26
FBA_D62 AD26
FBA_D63 AD27

FBA_DQM0 D23
FBA_DQM1 C26
FBA_DQM2 D19
FBA_DQM3 B19
FBA_DQM4 T24
FBA_DQM5 T26
FBA_DQM6 AA23
FBA_DQM7 AB27

FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
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FBA_DQS_RN0
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FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7

NB9M_GS

FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 E13
FBVDDQ_06 F13
FBVDDQ_07 F14
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H26
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L26
FBVDDQ_22 M19
FBVDDQ_23 M22
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 V22

FBA_CMD0 F26
FBA_CMD1 J24
FBA_CMD2 F25
FBA_CMD3 M23
FBA_CMD4 N27
FBA_CMD5 M27
FBA_CMD6 K26
FBA_CMD7 J25
FBA_CMD8 J27
FBA_CMD9 G26
FBA_CMD10 J23
FBA_CMD11 M25
FBA_CMD12 M27
FBA_CMD13 G25
FBA_CMD14 L24
FBA_CMD16 K24
FBA_CMD17 G22
FBA_CMD18 K25
FBA_CMD19 H22
FBA_CMD20 H24
FBA_CMD21 F27
FBA_CMD22 J26
FBA_CMD24 G24
FBA_CMD25 G27
FBA_CMD26 M24
FBA_CMD27 K22
FBA_CMD28 J22

FBA_A3
FBA_A0
FBA_A2
FBA_A1
FBE_A3
FBE_A4
FBE_A5
FBA_CS0#
FBA_WE#
FBA_BA0
FBA_CKE
FBA_ODT
FBE_A2
FBA_A12
FBA_RAS#
FBA_A10
FBA_BA1
FBA_A8
FBA_A9
FBA_A5
FBA_A7
FBA_A4
FBA_CAS#
FBA_A13
FBA_BA2
FBA_CLK0
FBA_CLK1
FBA_CLK1_N

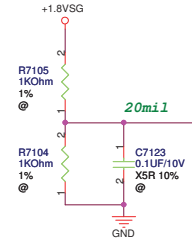
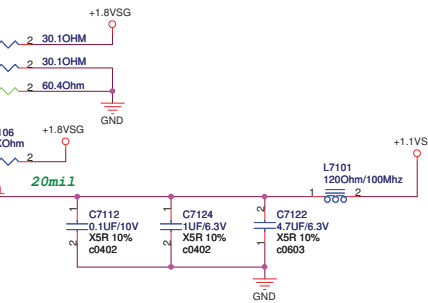
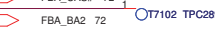
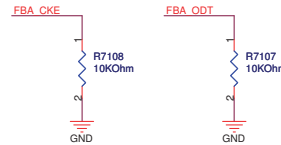
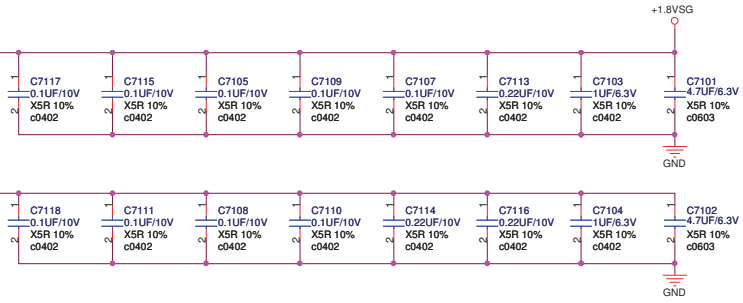
FBA_CLK0 F24
FBA_CLK1 F23
FBA_CLK1_N N23

FB_CAL_PD_VDDQ B15
FB_CAL_PU_GND A15
FB_CAL_TERM_GND B16

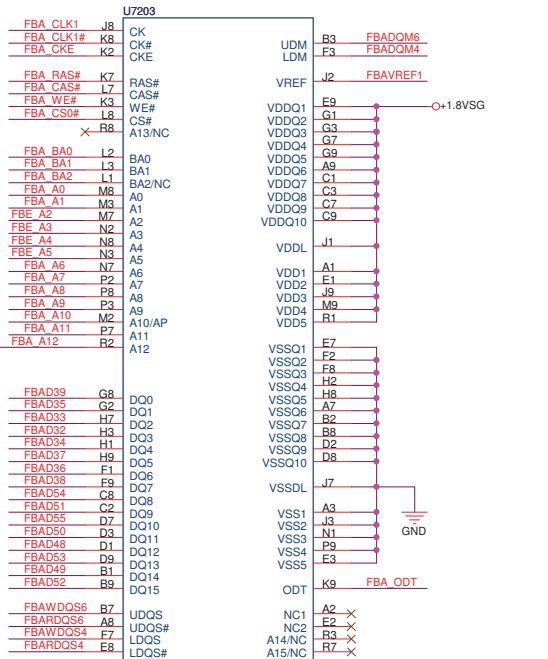
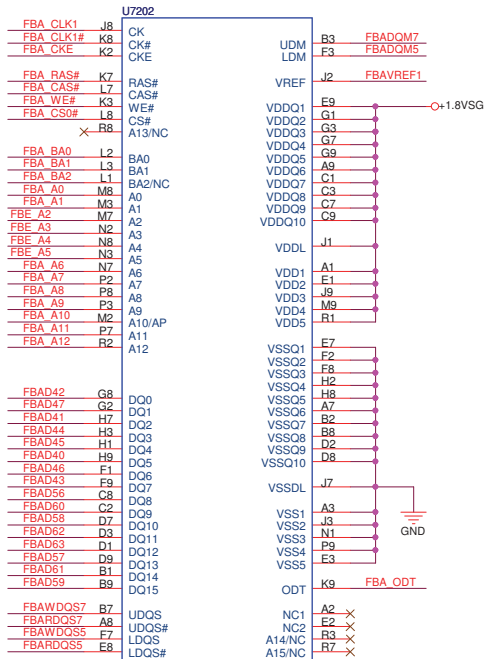
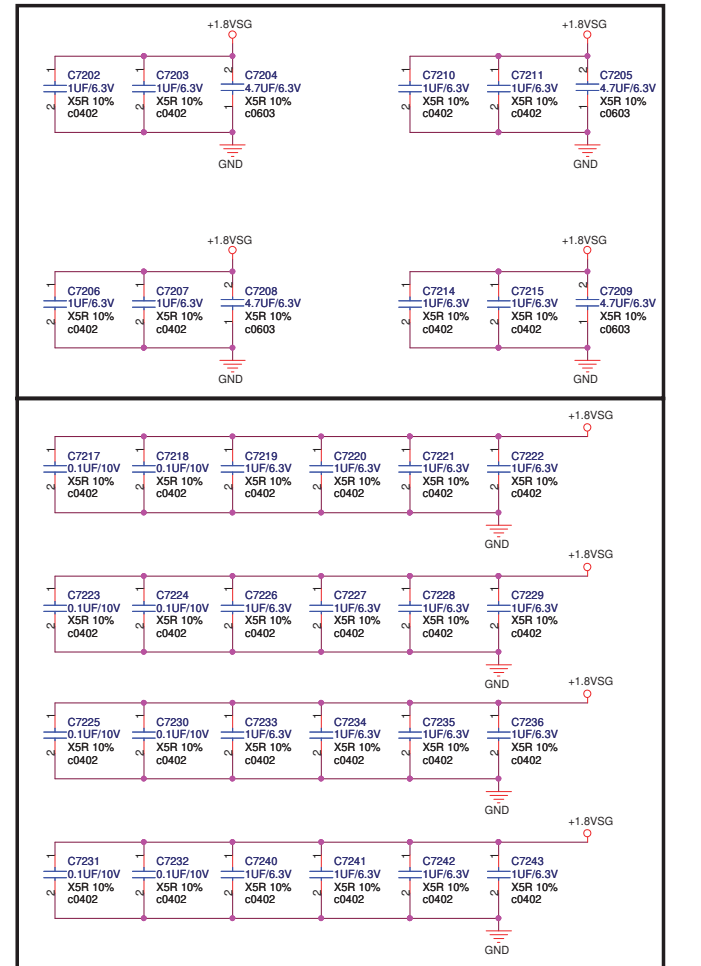
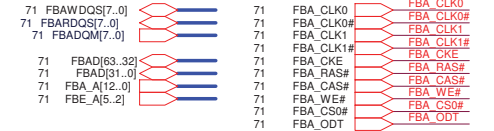
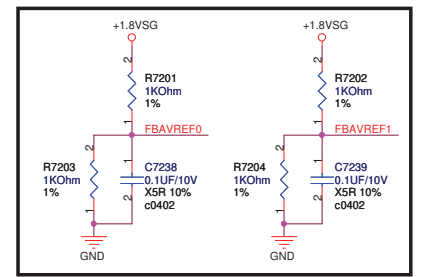
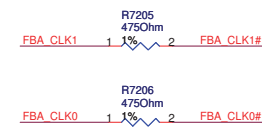
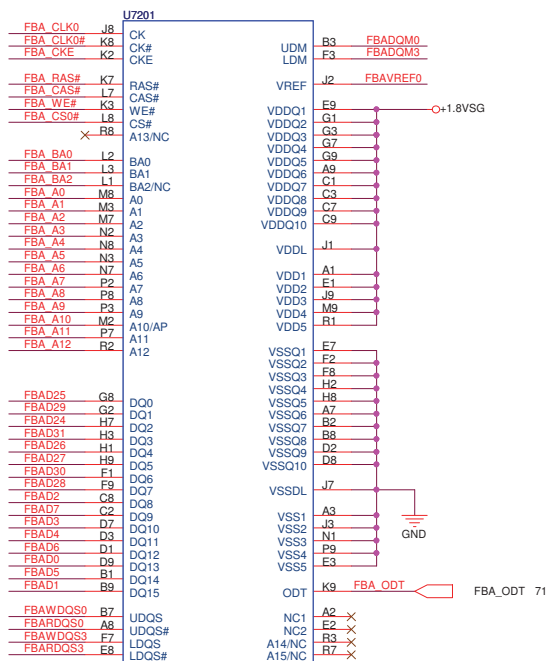
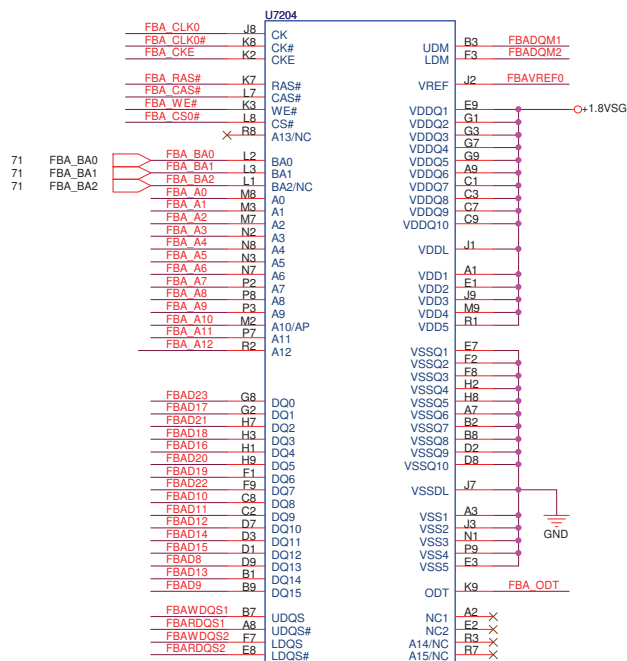
FBA_DEBUG M22

FB_PLLAVDD R19

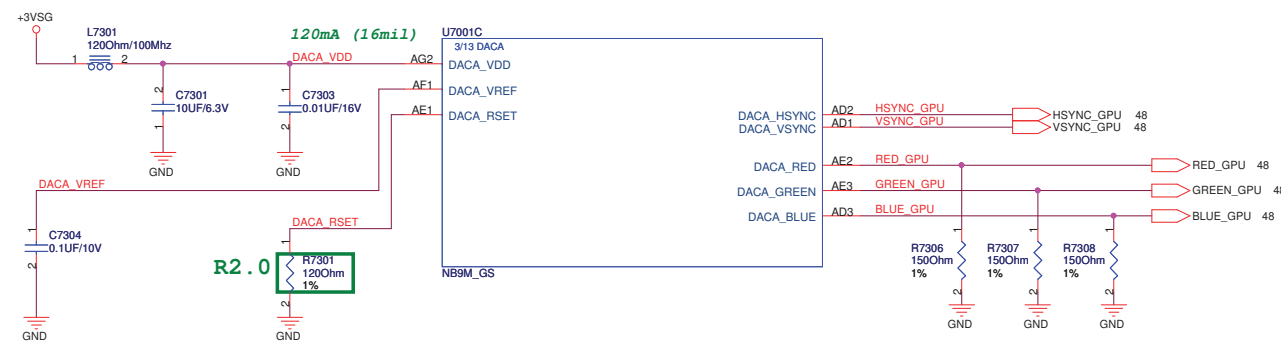
FB_DLLAVDD T19



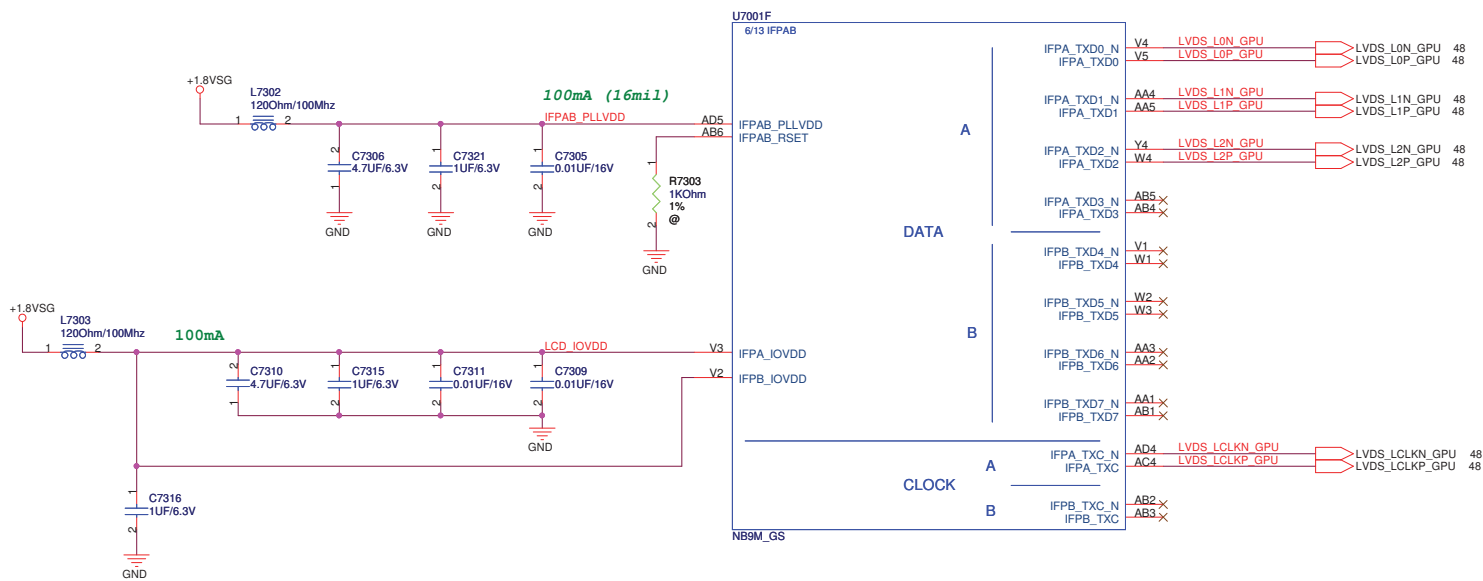
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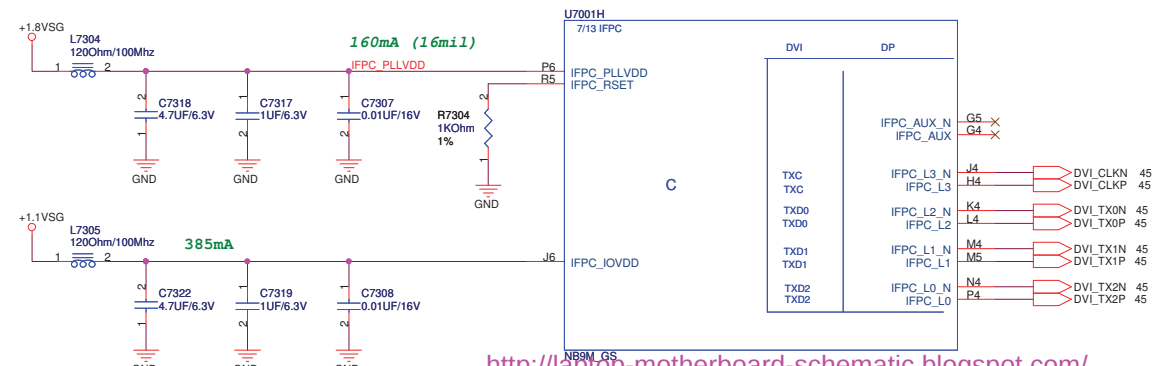
VGA



LVDS



HDMI



U7001I

10/13 HDAUDIO

HDA_BCLK A7-X

HDA_SYNC B7-X

HDA_SDI A6-X

HDA_SDO B6-X

HDA_RST_N C6-X

ACZ_RST#_HDMI_NV

NB9M_GS

R7305 10KOhm

GND

ASUS

ASUSTeK COMPUTER INC. NBI

Size Custom

Project Name **UX50**

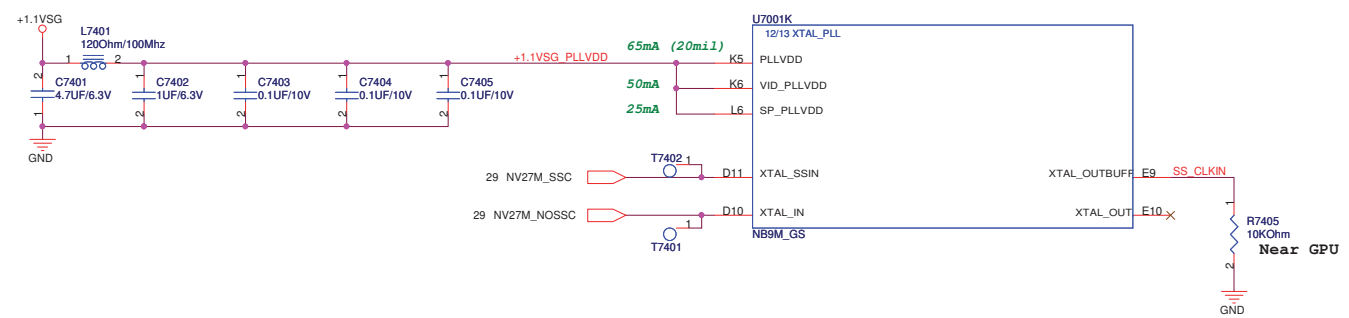
Date: Tuesday, March 31, 2009

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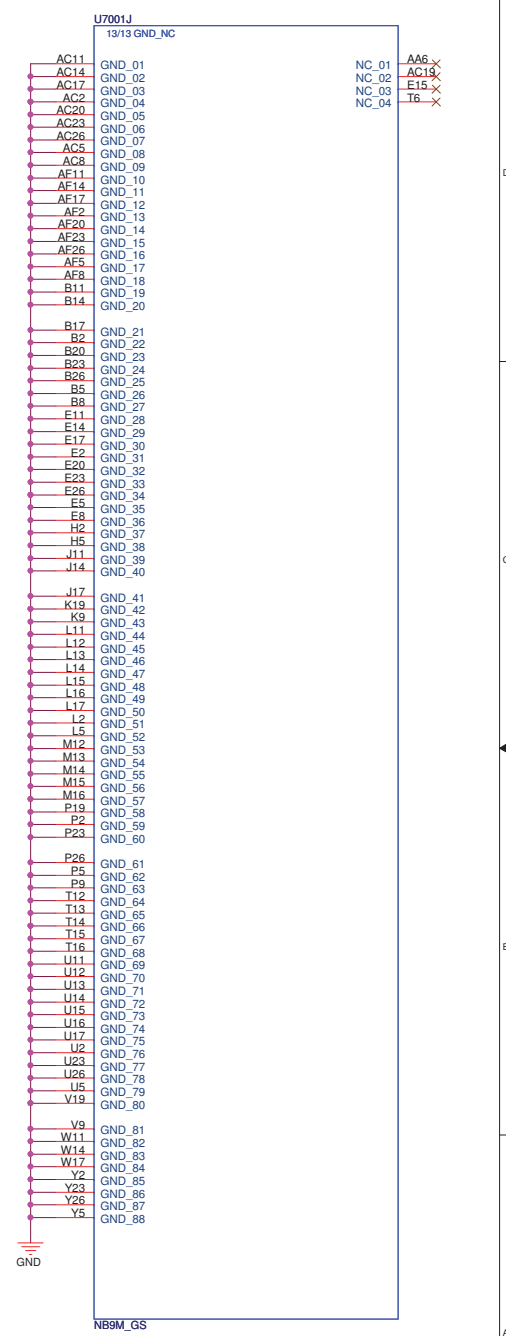
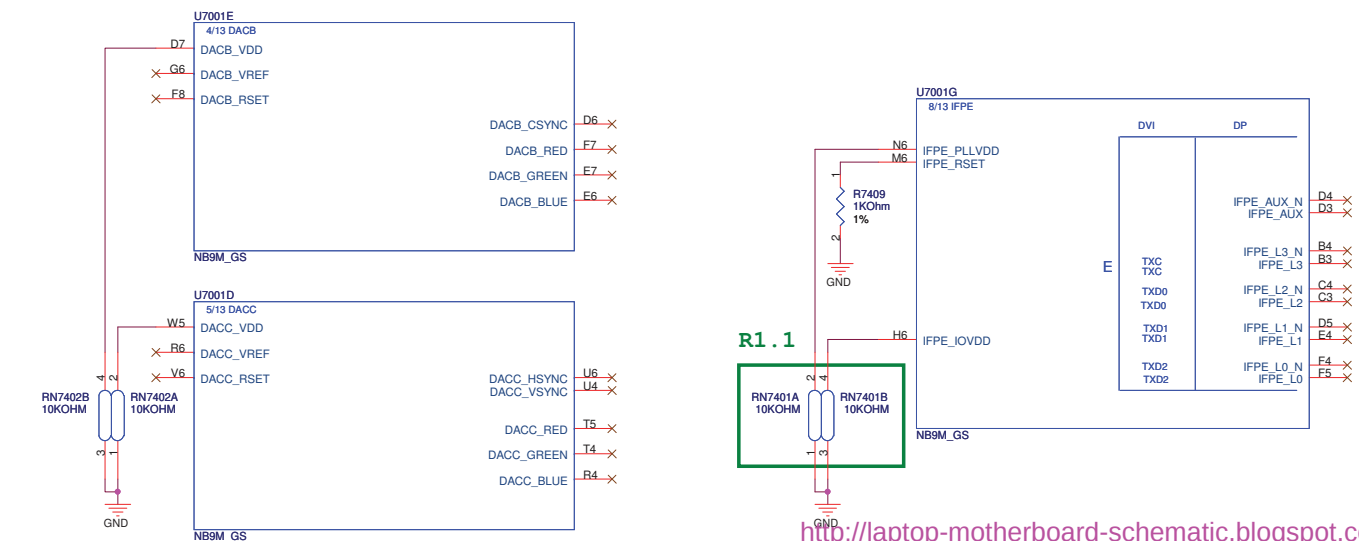
Rev 2.2

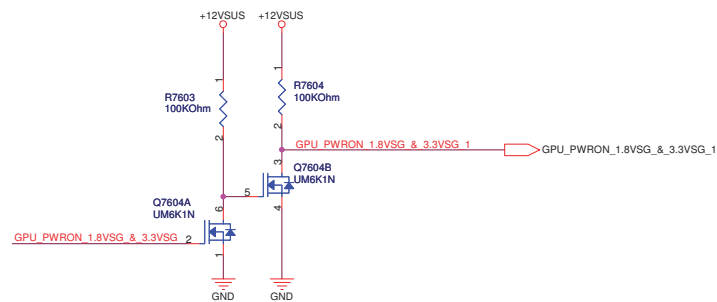
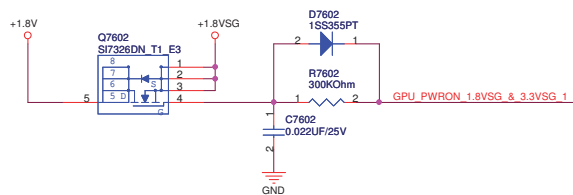
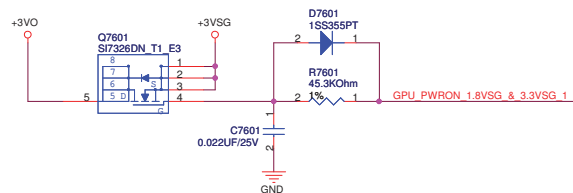
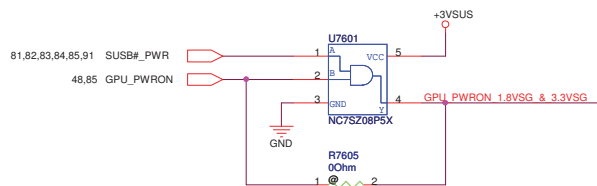
Title : Engineer: **Tony Su**

Xtal

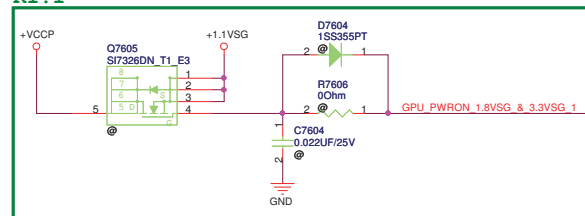


Other



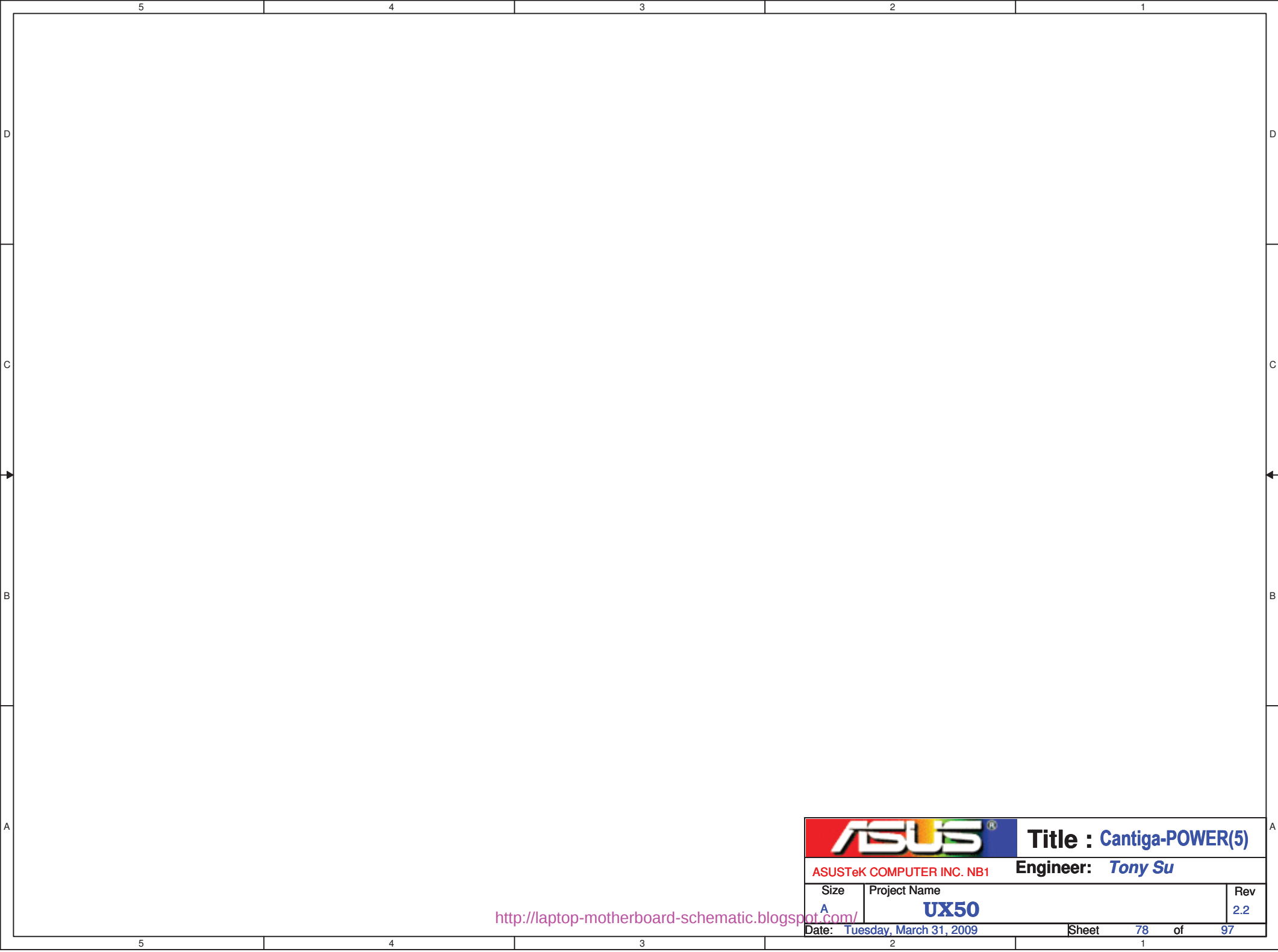


R1.1



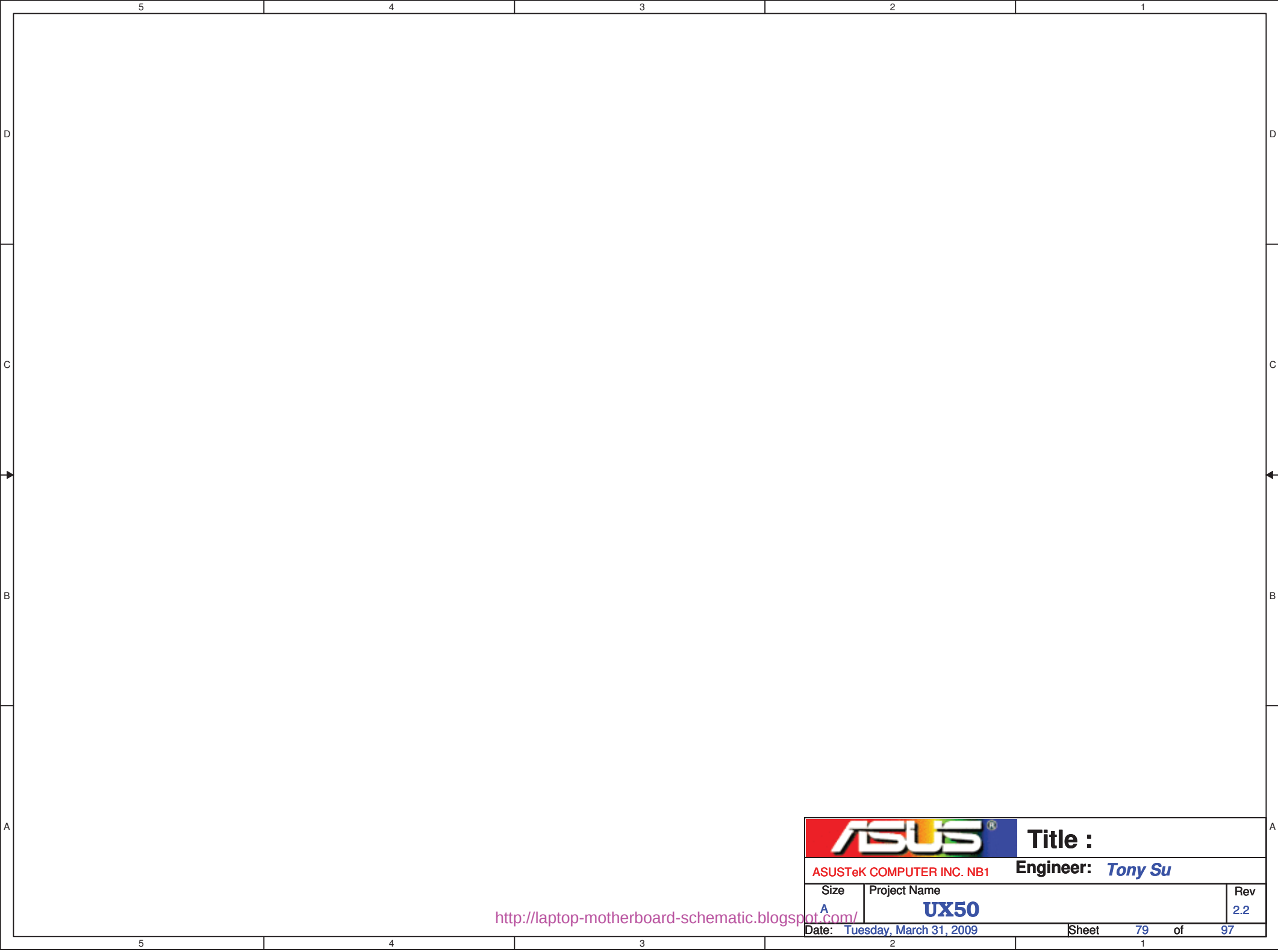


		Title : Cantiga-POWER(5)	
ASUSTeK COMPUTER INC. NB1		Engineer: Tony Su	
Size A	Project Name UX50		Rev 2.2
Date: Tuesday, March 31, 2009		Sheet 77 of 97	



		Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 2.2
Date: Tuesday, March 31, 2009		Sheet 78 of 97

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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
A	UX50		2.2
Date: Tuesday, March 31, 2009		Sheet	79 of 97



D

C

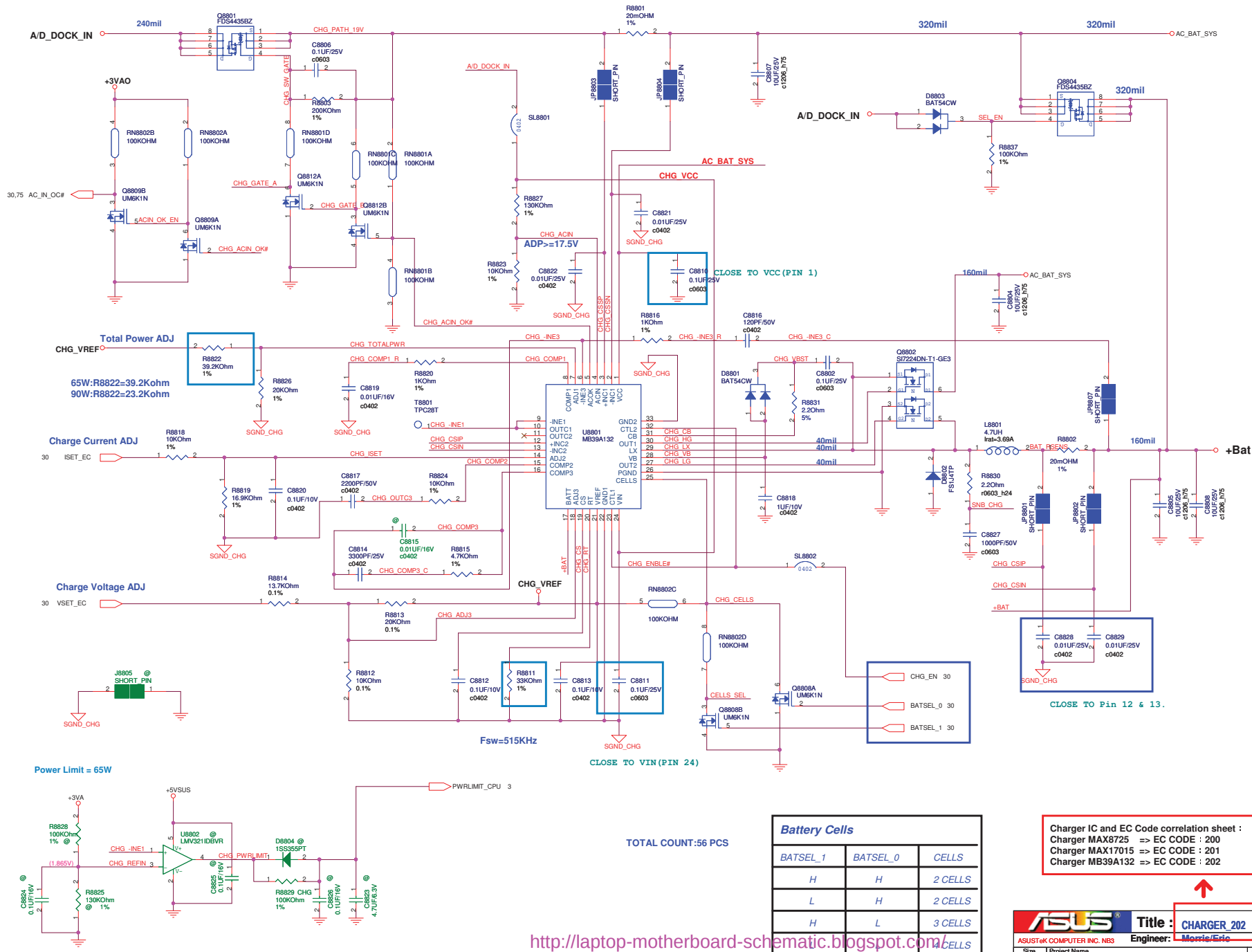
B

A

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Size	Document Number
A	<Doc>
Date:	Tuesday, March 31, 2009
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D

C

B

A

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Title	
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Size	Document Number
A	<Doc>
Date:	Tuesday, March 31, 2009
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BATTERY IN DETECT

<Variant Name>

**ASUS**

ASUSTeK COMPUTER INC. NB

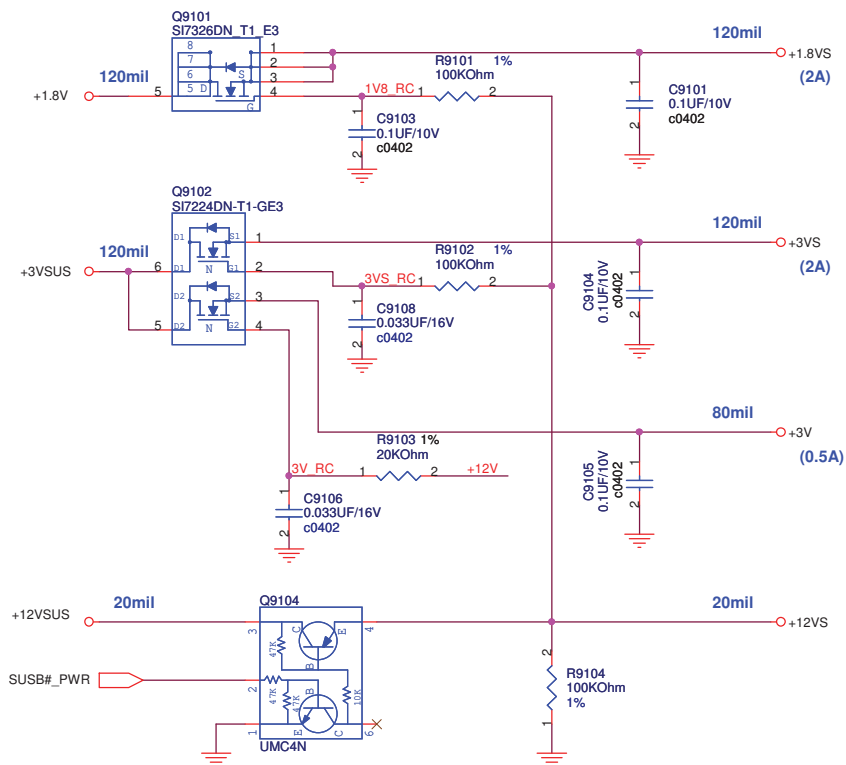
Title :POWER_DETECT

Engineer: Morris/Eric

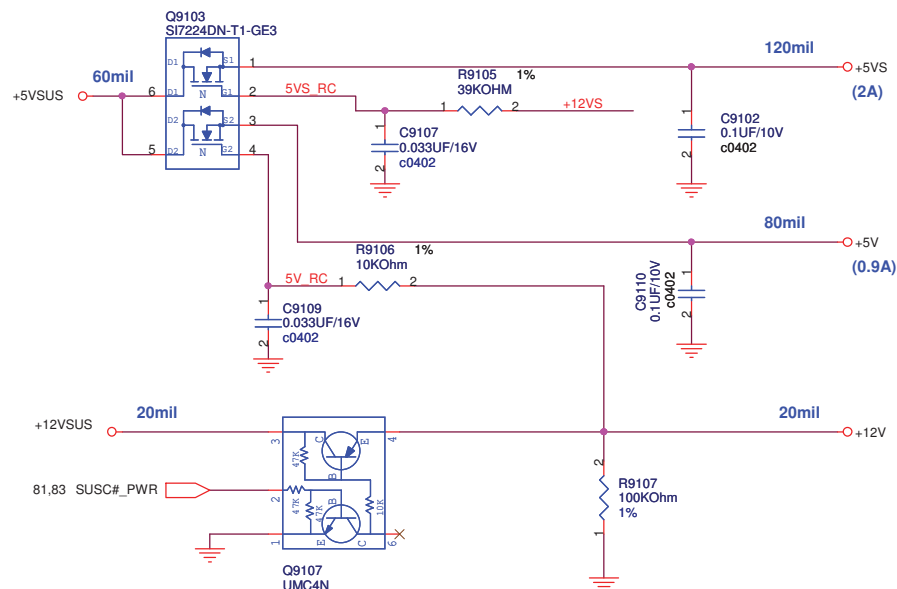
Size	Project Name	Rev
Custom	UX50	1.0

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SUSB#_PWR POWER



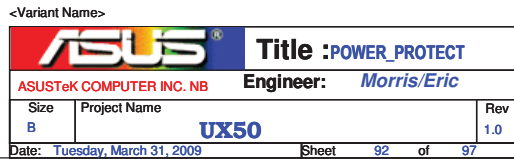
SUSC#_PWR POWER



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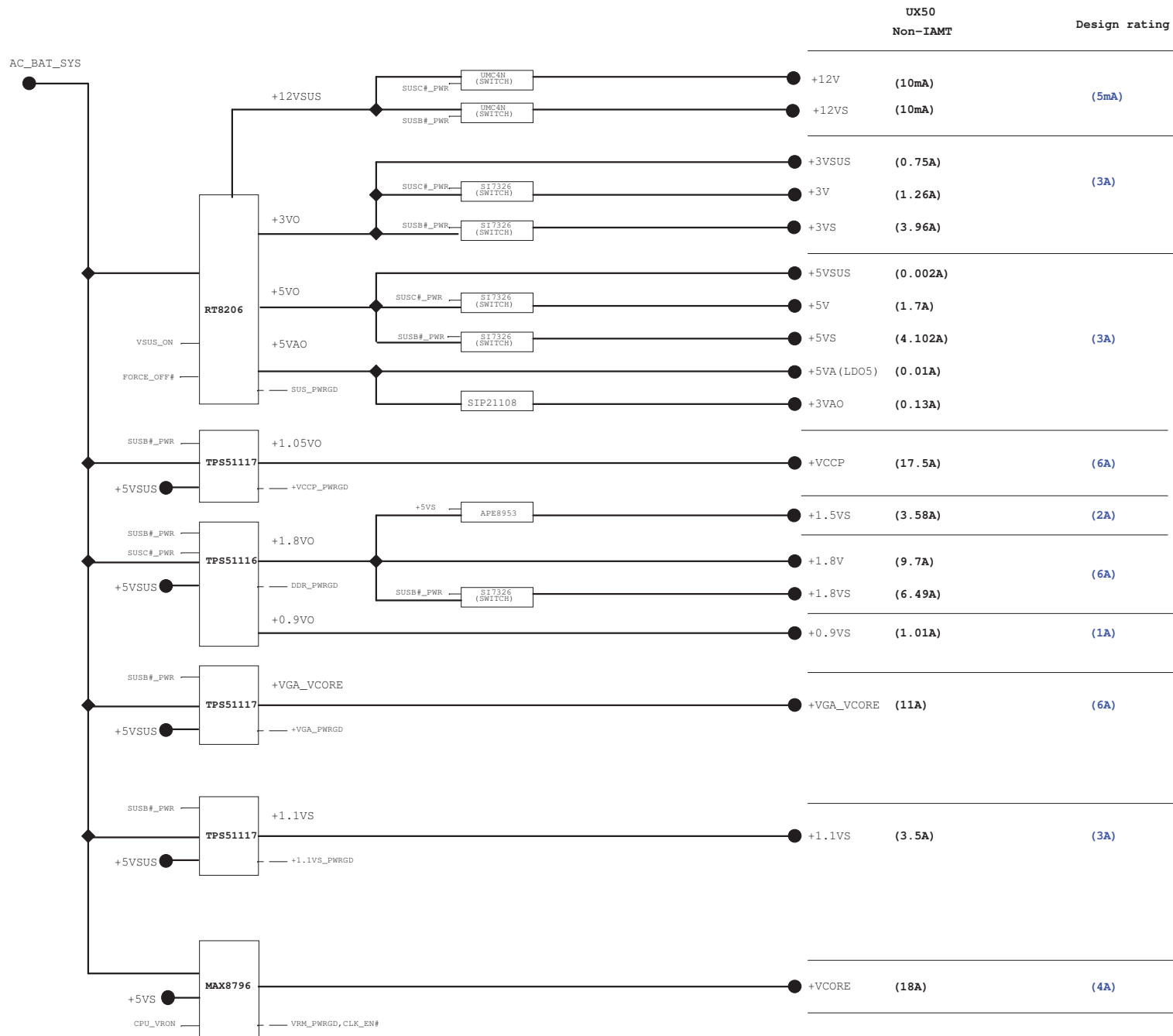
ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size B	Project Name UX50		Rev 1.0
Date: Tuesday, March 31, 2009		Sheet 91	of 97

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Total sum count: 236 pcs



VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLEPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON

<http://laptop-motherboard-schematic.blogspot.com/>



		Title :POWER_CHARGER	
ASUSTeK COMPUTER INC. NB3		Engineer: Eric_Ho	
Size	Project Name		Rev
A	UX50		1.0
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Rev	Date	Description
1.00		First Release!
1.10	02/08/2009	1. Change net ALS_AD to J6801. (Page 68) 2. Change RTC circuit from small board to M/B. (Page 20) 3. Add net CLK_PCIE_VGA and CLK_PCIE_VGA#.(Page 29) 4. Add pull-up for SMBus.(Page 22) 5. Add ITP connector. (Page 03,29) 6. Add MOS for dGPU power. (Page 76)
	02/10/2009	7. Change LAN PCIE to port 6. (Page 21) 8. Add AL_LED# to control ambient light LED. (Page 30,68) 9. Change C7036 to 4.7UF. (Page 70) 10. Swapping DDR2 nets (Page 09,29,74)
	02/11/2009	11. Add USB port for WiMax (Page 68,21) 12. Remove test point for layout. (Page 30)
	02/16/2009	13. Change 8pF cap for 32.768KHz crystal. (Page 20,30)
	02/17/2009	14. Swap J6801 BAT pins (Page 68)
2.00	03/04/2009	1. Remove D4503 for HDA issue. (Page 45)
	03/09/2009	2. Add HDMI hot plug detect in iGPU mode. (Page 48)
	03/09/2009	3. Add C6805 for EMI. (Page 68)
	03/12/2009	4. Change HDMI hot plug detect pin to EC GPI6. (Page 30,48)
	03/12/2009	5. Add CE0502 for CPU SU9600 hang issue. (Page 5)
	03/12/2009	6. Pull up backligh enable pin tto +3VS_LCD from +3VS. (Page 46)
	03/16/2009	7. Swap RN2917. (Page 29)
	03/18/2009	8. Change R7301 to 120ohm. (Page 73)

